Triggering in Particle Physics Experiments

IEEE Nuclear Science Sypmosium

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Peter J. Wilson - Fermilab

Course Introduction

Schedule

8:30 Trigger System Design

10:15 Break

10:45 Calorimeter and Muon based Triggers

12:15 Lunch

1:30 Track Trigger Processors

3:00 Break

3:30 Detached Vertex Triggers

Who We Are

Levan Bubakhadia (SUNY Stoneybrook)

- D0 Fiber Tracker and Preshower readout and Trigger

Sridhara Dasu (Univ of Wisconsin)

- CMS Level 1 Calorimeter Trigger

Giovanni Punzi (INFN – Pisa)

- CDF Silicon Vertex Trigger

Peter Wilson (Fermilab)

- CDF L1 and L2 Trigger Systems

Bias: hadron collider physics

Credits

- Material for this talk has come from many sources including:
  - Sridhara Dasu (CMS)
  - Wesley Smith (Zeus, CMS)
  - Gordon Watts (D0, general)
  - Levan Babukhadia (D0)
  - Erik Gottshalk (BTeV)
  - David Nitz (Auger)
  - Ted Liu (Babar)
  - LHC Electronics Workshop pages:

    http://lhc-electronics-workshop.web.cern.ch/LHC-electronics-workshop/

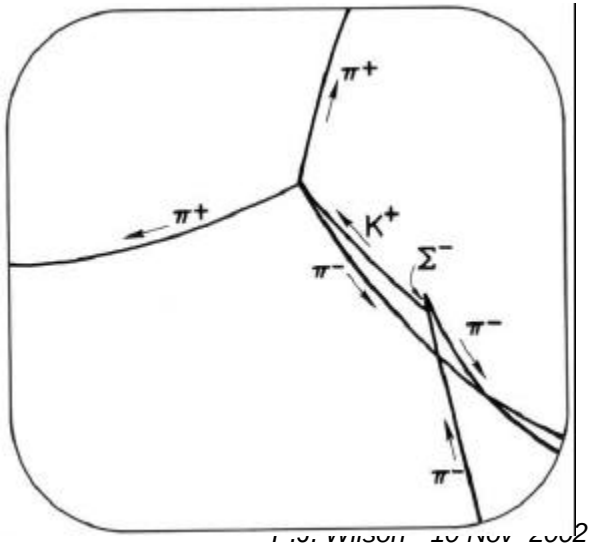
Why do you need a trigger?

- Select the interesting events of interest for further analysis.
- Rate of data accumulated in the experiment is too high to practically record directly to mass media
- Effort of storing and filtering the large volume of data is time consuming and expensive
- Need to make time stamp on readout or gate event
- Example: CDF and D0 for Run 2 at the Tevatron
  - Beam crossing rate = 7.6MHz (currently 1.7MHz)
  - About 750K channels at ~4 Bytes each = 3 Mbytes
  - Rate ~ 20 TeraBytes/Sec
  - Use zero suppression of unoccupied channels ➔ 250kB/event
  - Still rate ~ 2 TeraByte/sec
  - After the trigger, CDF or D0 Rate to tape ~ 20MB/sec!
  - Trigger rejects 99.999% of crossings! (at 1.7MHz only 99.997%)

Early Accelerator Expts: Bubble Chambers

- Bubble Chambers, Cloud Chambers, etc. (4π)
  - DAQ was a stereo photograph!
  - Effectively no Trigger:
    - Each expansion was photographed based on accelerator cycle
    - High level trigger was *human* (scanners).
  - Slow repetition rate.
    - Only most common processes were observed.
  - Some of the high repetition experiments (>40 Hz) had some attempt at triggering.

- Emulsions still used in some ν experiments (eg CHORUS, DONUT).
  - Events selected with electronically readout detectors $\Rightarrow$ scanning of emulsion seeded by external tracks



Early Fixed Target Triggers

1964 Cronin & Fitch CP Violation Experiment:

- K_2^0 mesons produced from 30 BeV protons bombarding Be target
- Two arm spectrometer with Spark Chambers, Cernkov counters and Trigger scintillators
- Spark chambers require fast (~20ns) HV pulse to develop spark, followed by triggering camera to photograph tracks
- Trigger on coincidence of Scintillators and Water Cerenkov counters
- Only one trigger level
- Deadtime incurred while film advances

Detector Layout of K_2^0 ® pp Experiment of Cronin and Fitch (1964)

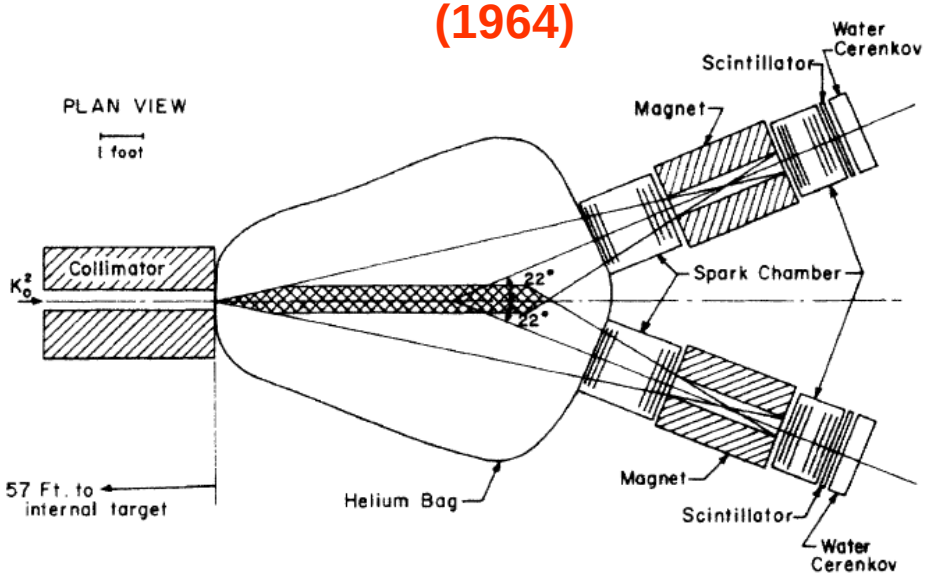


FIG. 1. Plan view of the detector arrangement.

Christenson, Cronin, Fitch and Turlay **PRL 13**, 138 (1964)

System Design Constraints

Experimental Constraints

Different experiments have very different trigger requirements due to operating environments

- Timing structure of beam
- Rate of producing physics signals of interest
- Rate of producing backgrounds

- Cosmic Ray Expts – no periodic timing structure, background/calibration source for many other experiments.
- Fixed Target Expts – close spacing between bunches in train which comes at low rep rate (~Hz)
  - Backgrounds from un-desirable spray from target
  - Cosmics are particularly a background for neutrino beams
- e+e- collider – very close bunch spacing (few nsec), beam gas and beam wall collisions
- ep collider – short bunch spacing (96ns), beam gas backgrounds
- pp/ppbar collider – modest bunch spacing (25-400ns), low produced soft QCD

Cross-sections and Luminosity

- Standard method of characterizing rates is:

  Rate = σ **L**

  σ - cross-section (units of cm^2 or barn=$10^{24}cm^2$), probability that an interaction will occur. If this were a game of darts, the larger the area of the dart board the more likely you will get the dart on the board.

  L - luminosity (units of $cm^{-2}s^{-1}$ or $barn^{-1}\ sec^{-1}$), cross sectional density of the beams. The more particles per beam or the more compact (transverse) the higher the luminosity. For colliding beam, goes as the product of the two beam currents.

Convenient conversion: $L = 10^{30}cm^{-2}s^{-1} = 1mb^{-1}s^{-1}$

Cross Sections for e+e-

- At Ecm=10.6 GeV B-Factories

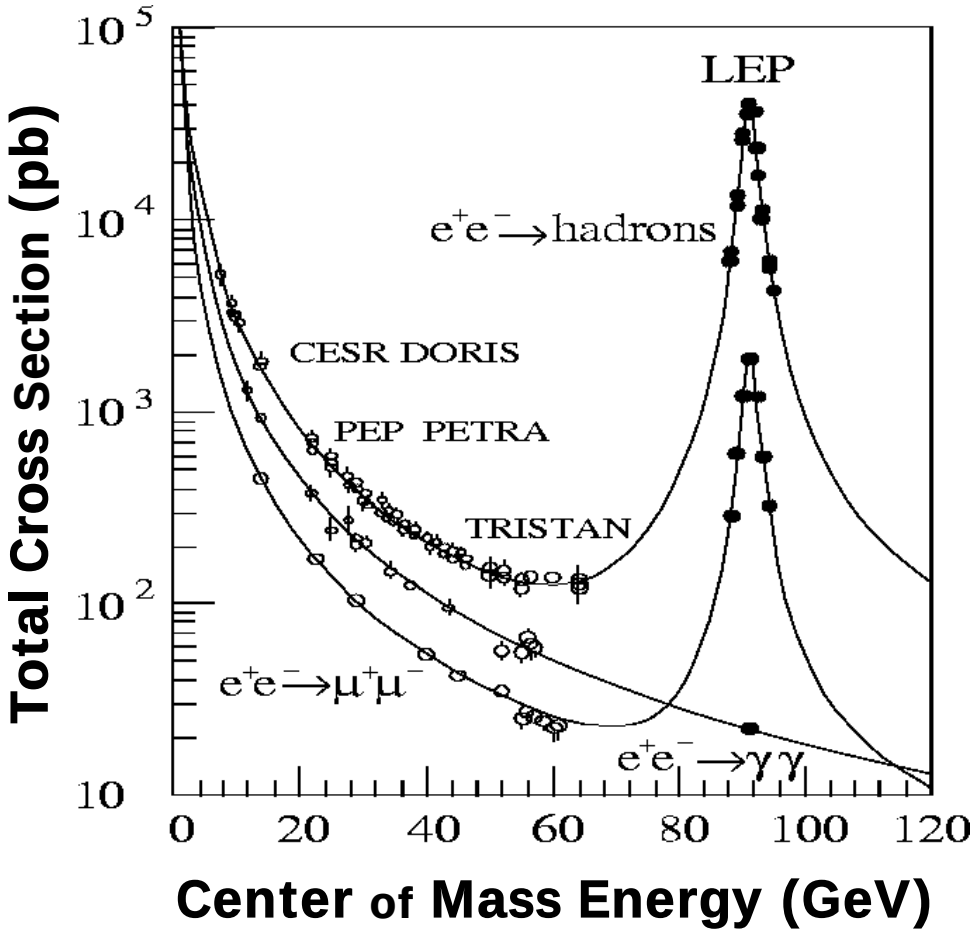
(from CLEO III)

	s(Tot) (nb)	s(Barrel) (nb)	s(Endcap) (nb)
e+e– → e+e–	72	19	53
e+e– → γγ	6.2	3.7	2.5
e+e– → μ+μ–	0.72	0.60	0.12
e+e– → τ+τ–	0.72	0.60	0.12
e+e– → hadrons	4		
Total	84		

Total rates of few hundred Hz at current luminosities

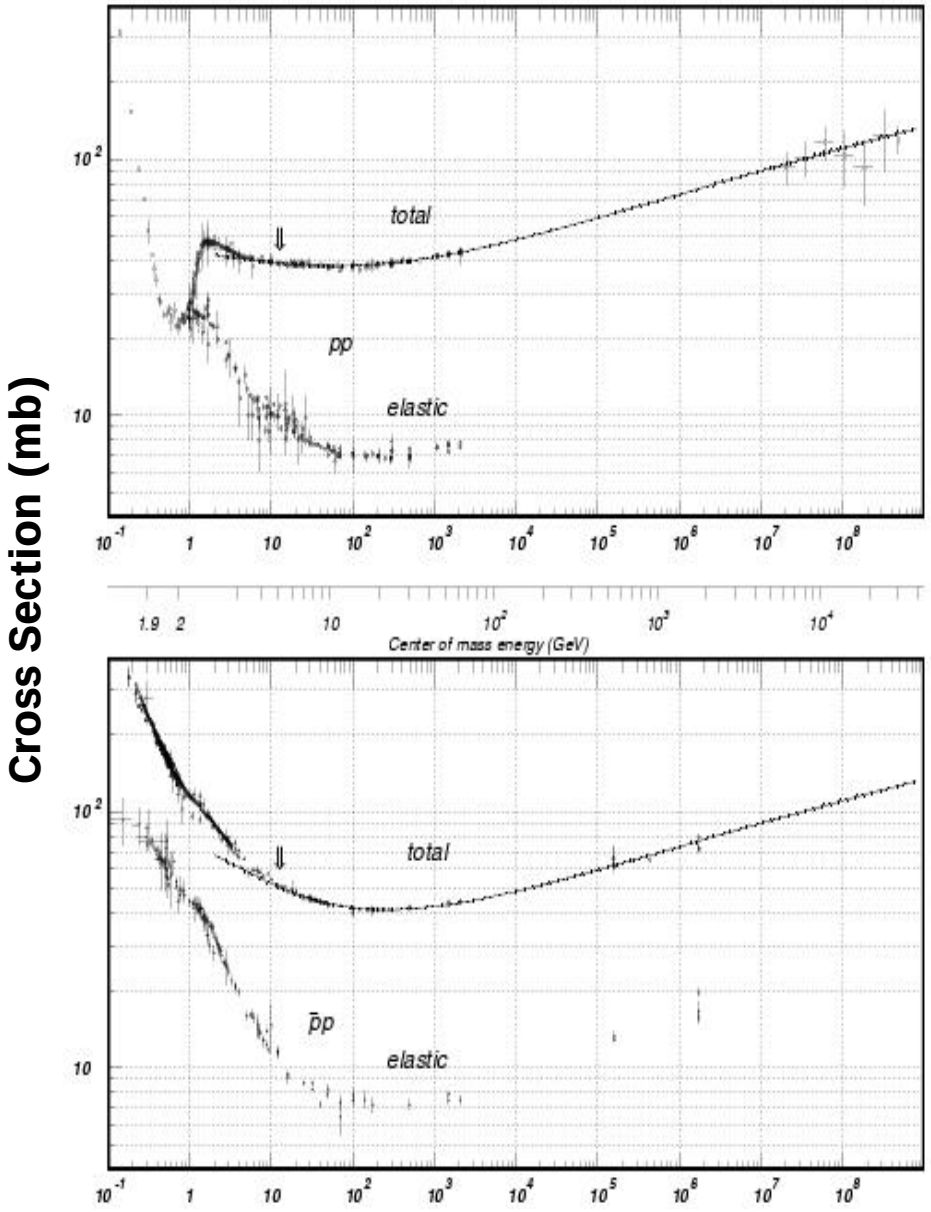
- At Ecm = 90 GeV (LEP, SLC on Z-boson)
  - 30nb to hadrons
  - 2nb to τ+τ– or μ+μ–

Total rates of 5-10 Hz at LEP and LEPII



Cross Sections for $pp/p\bar{p}$

- $p\bar{p}$ Cross Section at 1960 GeV (Tevatron)
  - About 50mb
  - Dominated by inelastic scattering
  - At Run 2 luminosities: interaction rate is 2-20MHz
- pp Cross Section at 14TeV (LHC)
  - About 70mb
  - Dominated by inelastic scattering
  - At LHC design luminosity: interaction rate close to 1GHz



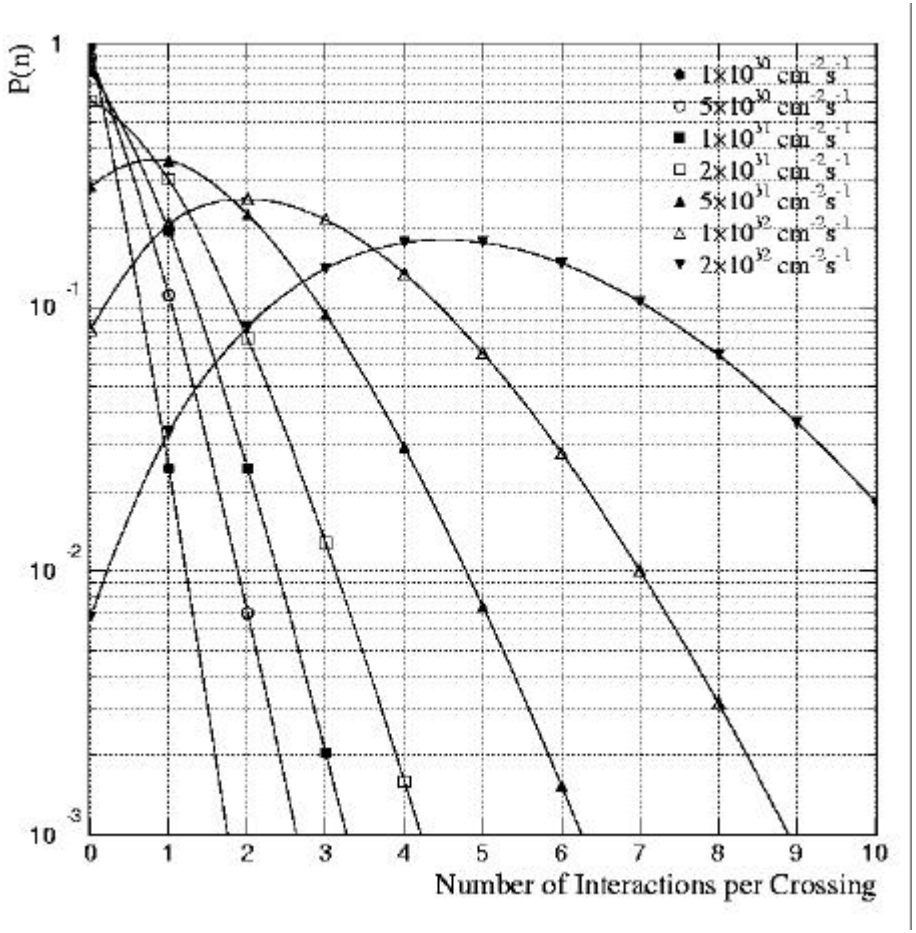
Multiple Interactions

- For hadron colliders (and some fixed target expts) the interaction rate exceeds the machine bunch spacing causing multiple interactions per crossing:

  $\mu = <\text{Inter/X-ing}>$

  $= \sigma * \mathbf{L} \ / \ \text{Crossing Rate}$

- The number of interactions for each crossing is poisson distributed about the mean μ



Colliding Beam Machines

Accelerator	Type	Energy (GeV)	Bunch Spacing	Luminosity ($\mu b^{-1} s^{-1}$)	Int. per Crossing
CESR (CLEO)	e+e-	10.6 (3-4)	14	1280	$\sim 10^{-5}$
KEKB (Belle)	e+e-	10.6(3.5x8)	8 (2)	8256	$\sim 10^{-5}$
PEP-II (Babar)	e+e-	10.6(3.1x9)	4.2	4600	$\sim 10^{-5}$
LEP (Aleph, Opal, Delphi, L3)	e+e-	90-210	22,000	24-100	$\sim 10^{-3}$
HERA (H1, Zeus)	ep	27x920	96	75	<<1
Tevatron (CDF, D0, BTeV)	$p\bar{p}$	1960	396(132)	36(200-500)	1(3-10)
LHC (Atlas, CMS, LHCb, Alice)	pp	14,000	25	10,000	25

PDG 2002: K. Hagiwara et al., Phys. Rev. **D 66**, 010001 (2002) or http://pdg.lbl.gov and experiment web sites

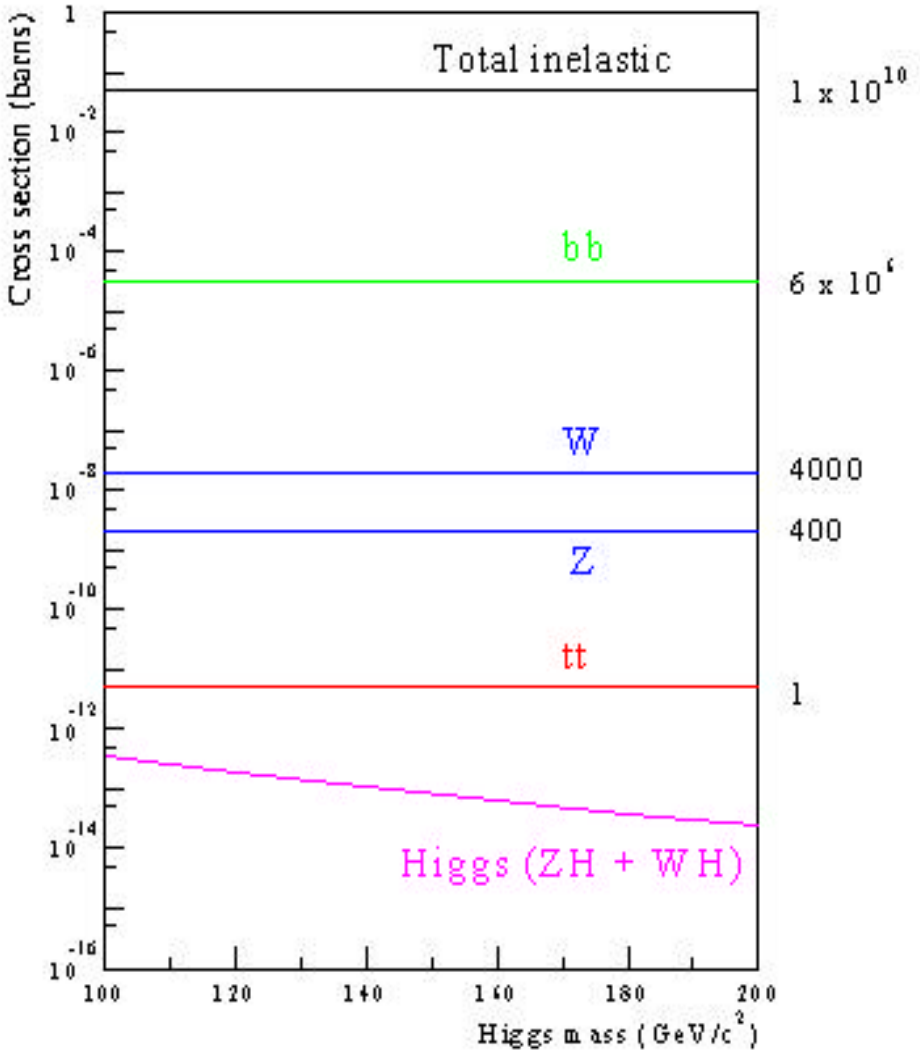
For e+e- and ep machines, cross sections are small and multiple interactions are negligible at all current machines

- For e+e- even pileup in slow detectors (~1μs) not a large problem
- At HERA beam-gas background (50-100kHz) can be problem

For hadron colliders: multiple interactions are a major issue for detector design, particularly tracking chambers, DAQ and Trigger

Particle Spectrum in pp

- Cross sections for particle production vary by a factor of ~ 10^{10} (diffraction to Higgs)
- Spectrum is similar for Higher Energy machine (eg LHC) except higher mass particles are more accessible
- Triggering challenge is to reject low P_T/Mass objects while keeping high P_T/mass
- Of course CDF, D0 and particularly BTeV and LHCb want to keep a large fraction of b events as well so need to se



Efficiency and Dead-time

Goal of Trigger and DAQ is to maximize data for desired process to storage for analysis with minimal cost

$$\varepsilon = \varepsilon_{\textbf{operations}} * \varepsilon_{\text{trigger}} * (1\text{-deadtime})$$

- Relevant efficiency is for events that will be useful for later analyis:

$$\varepsilon_{\text{trigger}} = \text{Ngood(accepted)}/\text{Ngood(Produced)}$$

- Low rate process (eg e+e- ➔ hadrons, Higgs production at Tevatron or LHC), try to accept all in trigger ⇨ Maximize efficiency
- Deadtime incurred do to fluctuations when rate into a stage of trigger (or readout) approaches the rate it can handle. Simple case of no buffering:

$$\textbf{Dead-time} = (\text{Rate In}) * (\text{Execution Time})$$

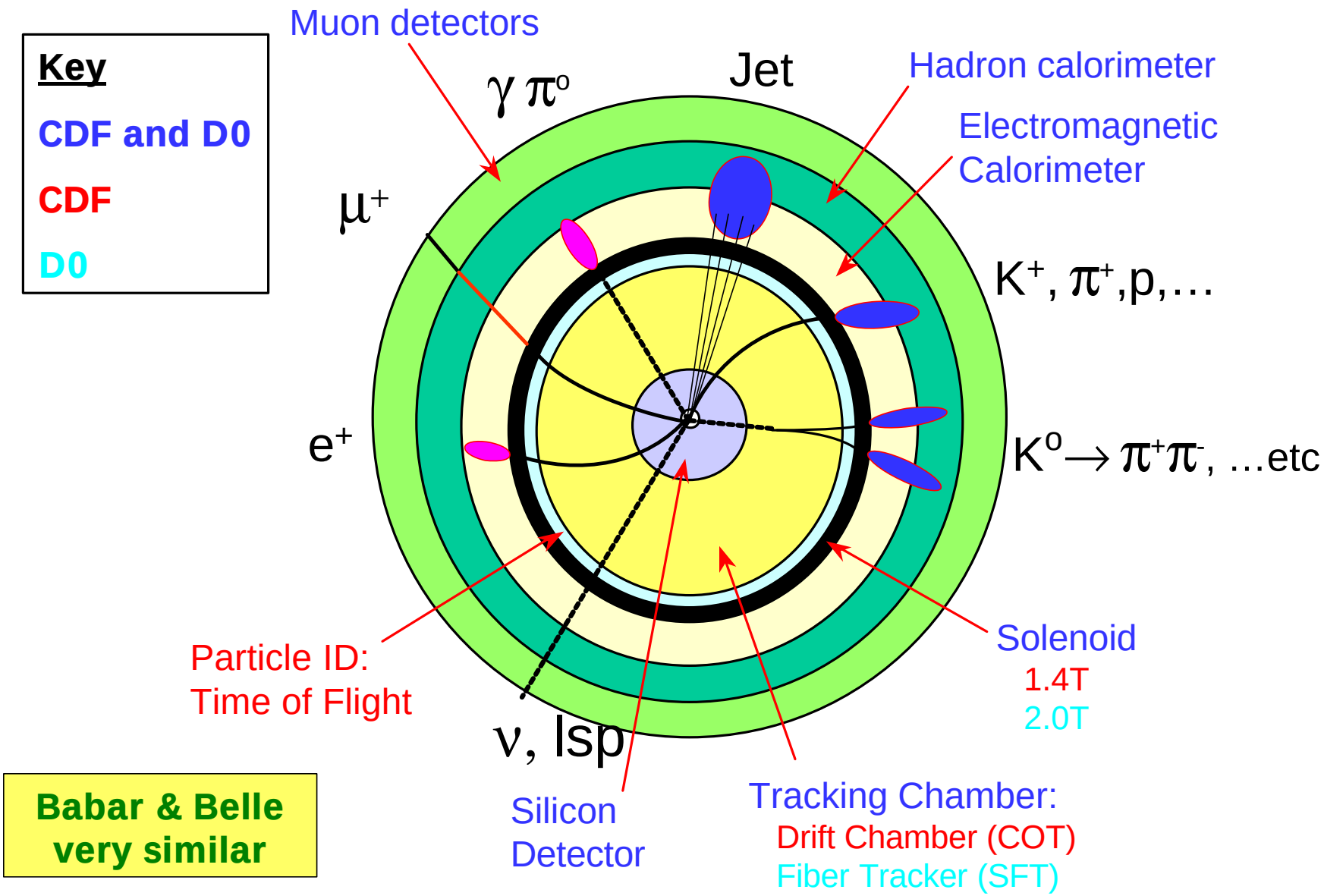
- Buffering incoming data reduces dead time, more buffering less dead time
  - If <Incoming Rate> > 1/<Execution Time>, dead no matter what!
- Minimizing dead-time helps all processes
  - 1% of machine time * 1 year = $$$$$

Efficiency and Dead Time (2)

- Need to ensure full efficiency when detector channels are broken, masking registers are used at the input from front-ends
  - For tracking mask on dead channels
  - For calorimeter mask off hot channels
- Need precise measurements of $\varepsilon_{trigger}$ and dead-time for cross-section (hence production limit) measurements
  - Other cases (eg particle lifetime) need to evaluate other biases that trigger may introduce (eg removing long lived decays)
- Measure dead time by scaling rates of operational states of Trigger/DAQ system
- Need Mechanisms to evaluate the efficiency and biases
  - Redundant, independent paths
  - Lower bias triggers with accepted with a pre-scale
  - Zero bias - trigger on accelerator clock structure
  - Minimum bias – trigger on very low energy scattering

Signatures in Detectors

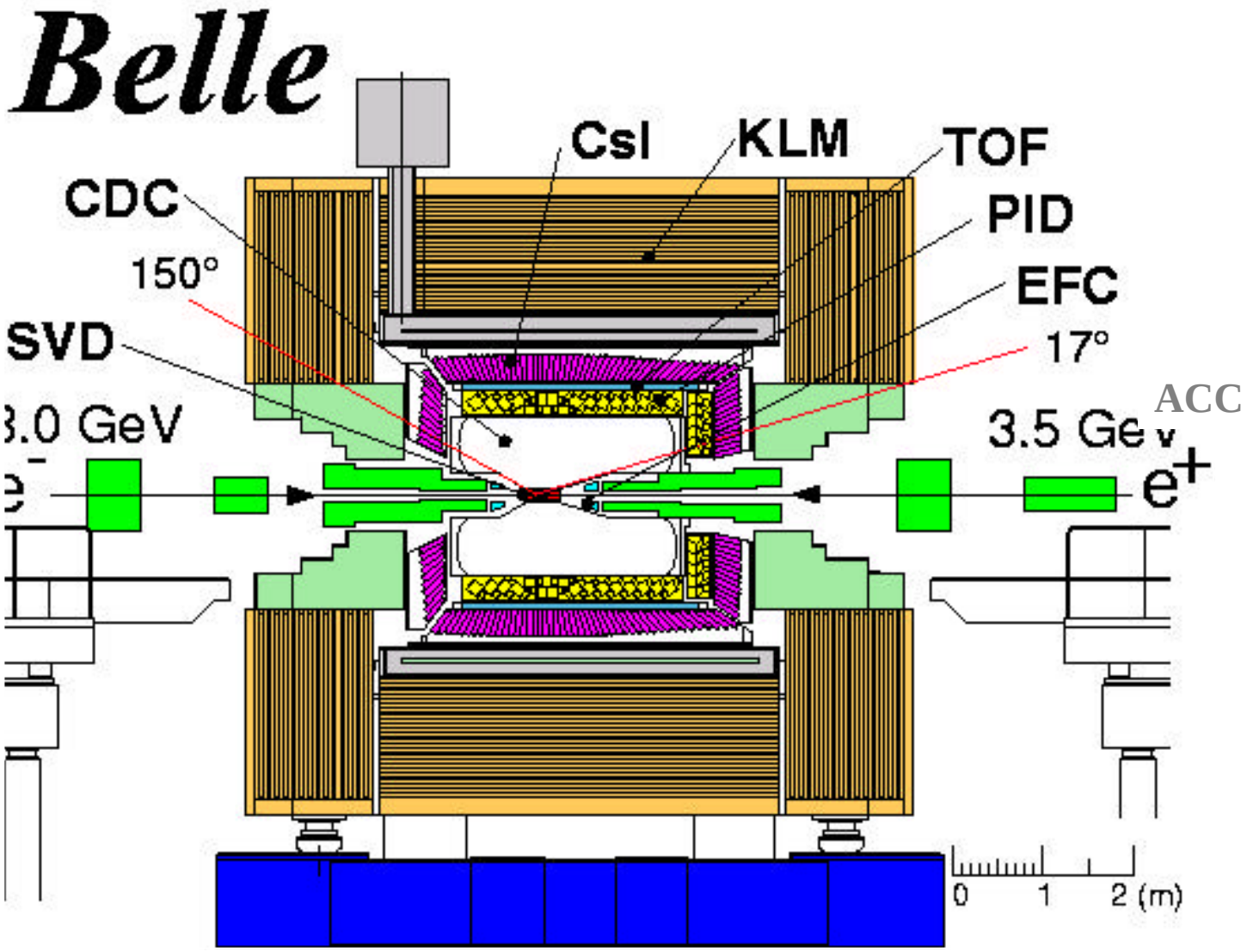
Collider Detector Schematic



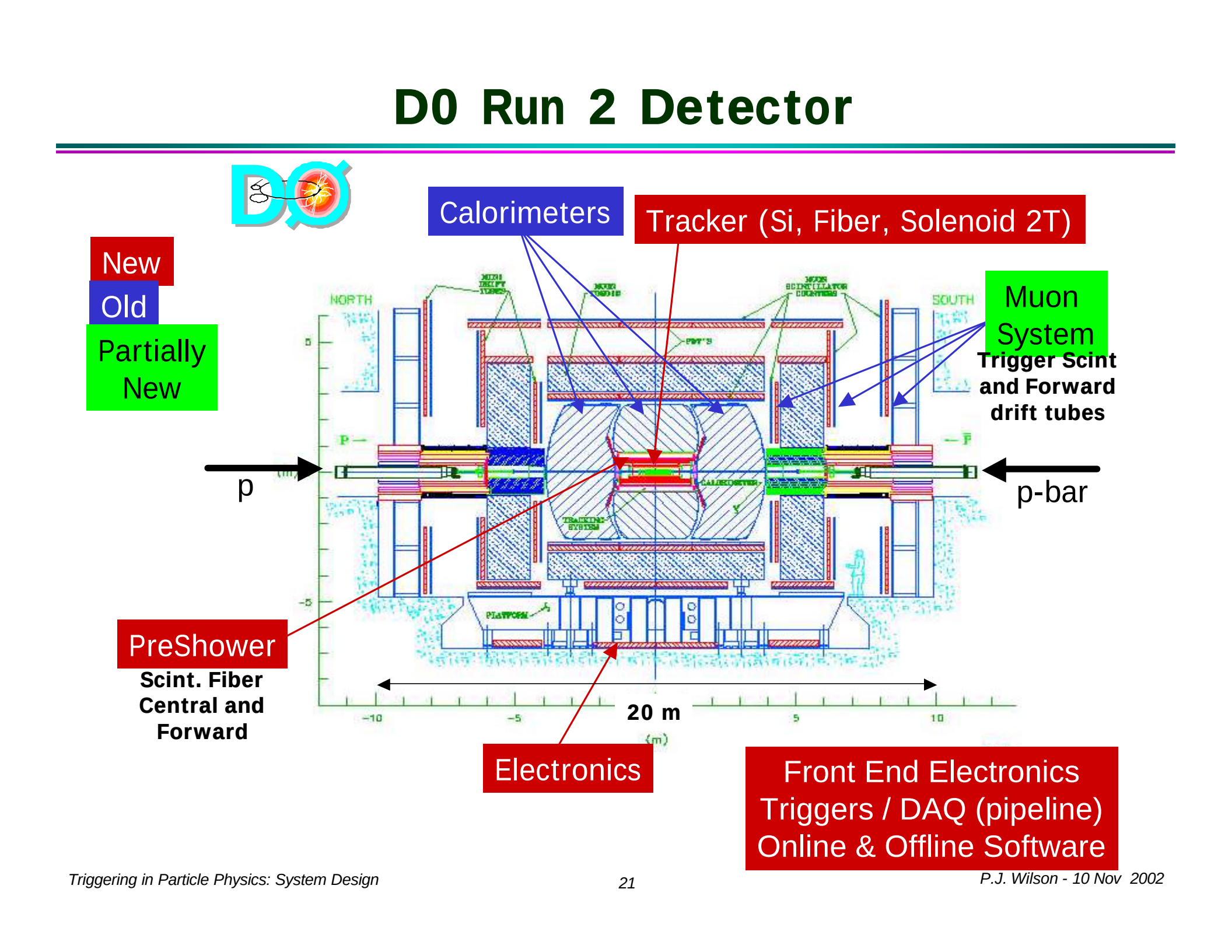
Recent Collider Detectors

Detector	Number of Channels	Silicon Part of Trigger?	Input Trigger Rate	Largest (Non) Physics Background
CLEO III	400K	No	L1: 72 MHz L2: 1 kHz Tape: <100 Hz	Electron pairs & $\gamma\gamma$
Belle	150K	Not Yet	L1: 50 MHz L2: 500 Hz Tape: 100 Hz	Electron pairs & $\gamma\gamma$ Beam-wall
BaBar	150K	No	L1: 25 MHz L3: 2 kHz Tape: 100 Hz	Electron Pairs & $\gamma\gamma$ Beam-Wall
H1, ZEUS	500K	No	L1: 10 MHz L2: 1 kHz L3: 100 Hz Tape: 2-4 Hz	Beam-gas
HERA-B	600K	Yes (L2)	L1: 10 MHz L2: 50 kHz L3: 500 Hz L4: 50 Hz Tape: 2 Hz	Beam-wire scattering Inelastics
Aleph, Opal, L3, Delphi	250-500k	No	L1: 45 kHz Tape: 15 Hz	Beam-gas
CDF (Run 2), **DØ** (Run 2)	750K-1M	Yes (L2)	L1: 7 MHz L2: 10-50 kHz L3: .3-1 kHz Tape: 50 Hz	QCD, pileup (multiple interactions)

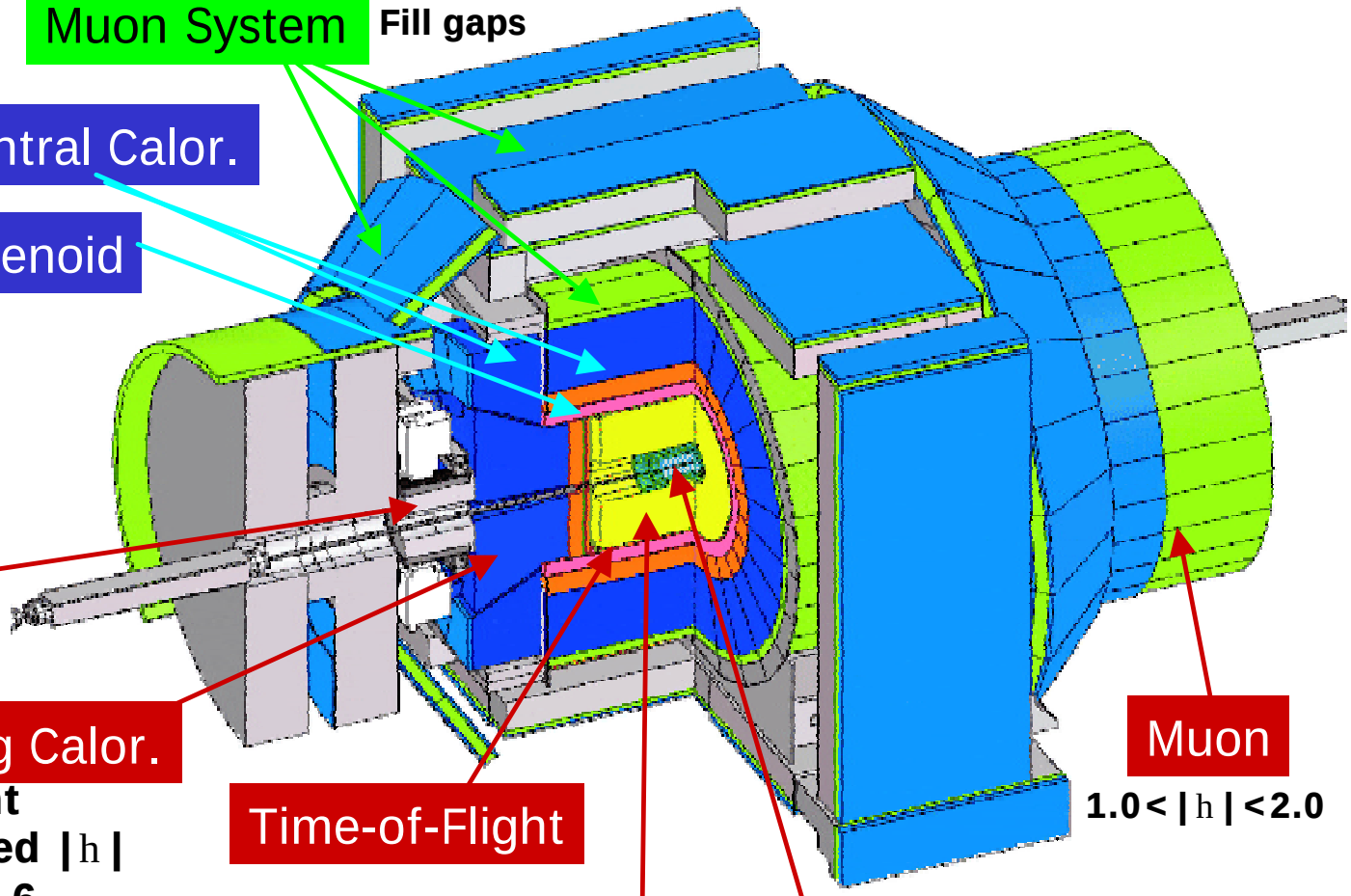
Belle Detector



D0 Run 2 Detector



CDF II Detector



Front End Electronics
Triggers / DAQ (pipeline)
Online & Offline Software

Requirements for e+e- Triggering

Accept: (almost) all real collisions

Reject:

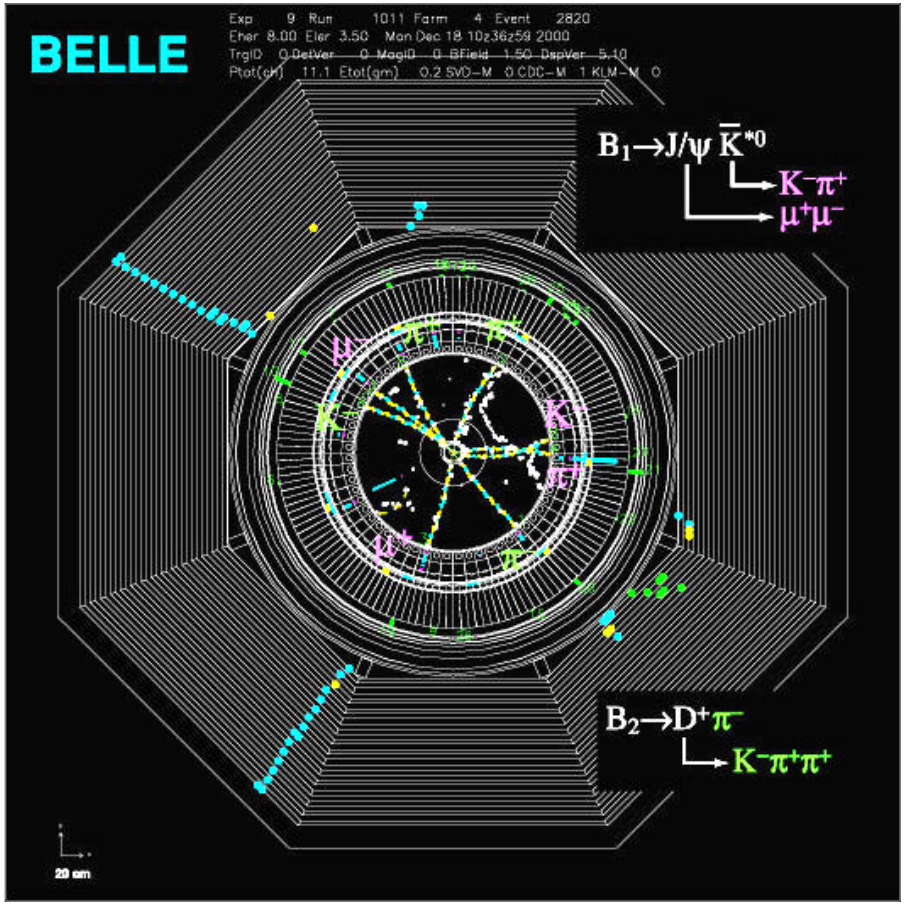
- very low angle e+e-
- Beam-gas/wall events - tracks not from beam spot in r or z

Trigger on simple event topology

- Time-Of-Flight coincidence
- Multiplicity of good tracks (from beam spot) – low pt cuts (100s of MeV/c)
- Calorimeter activity: global energy and clustered energy in relative coarse spatial bins
- Simple combinations

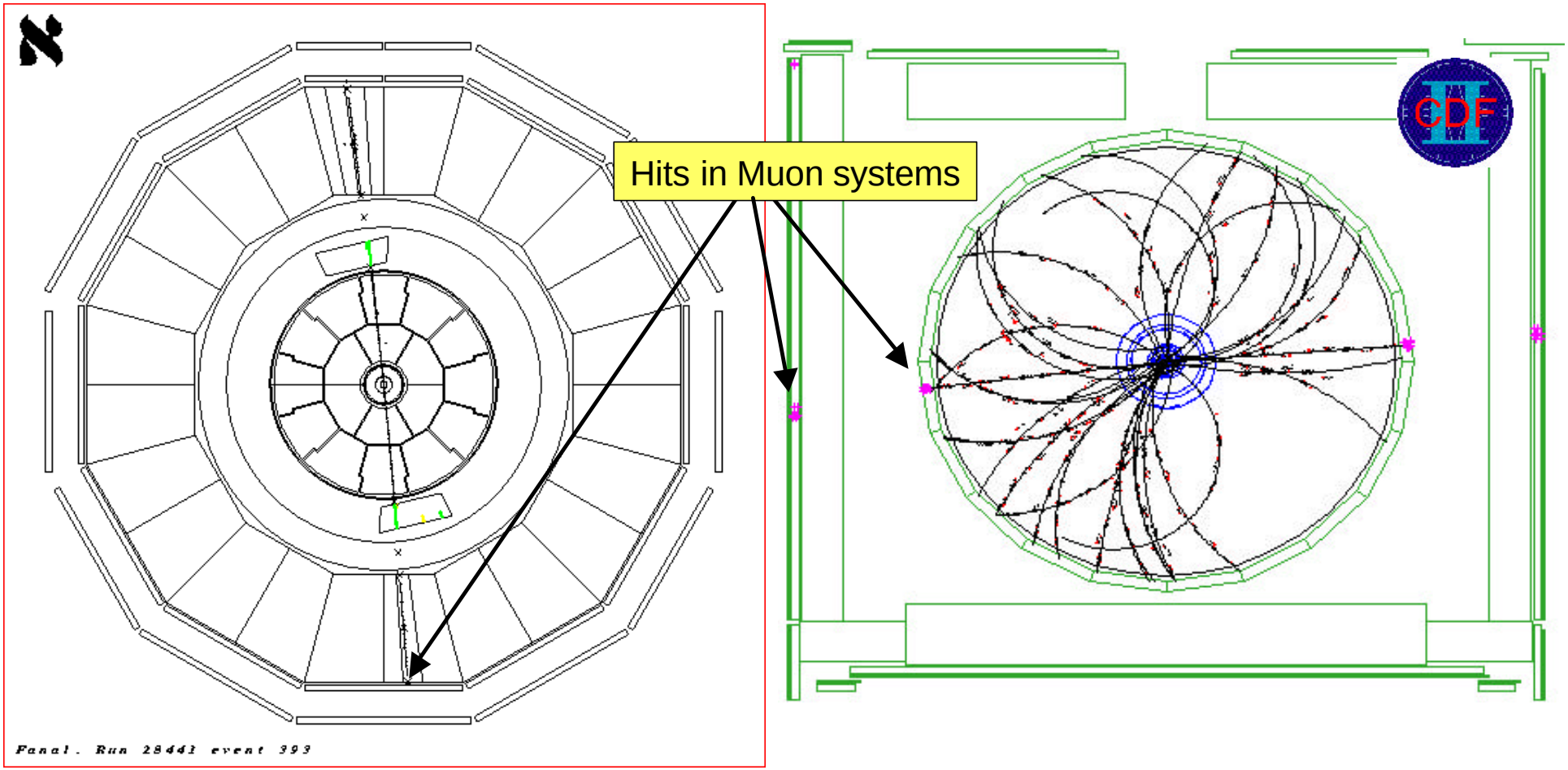
Time stamping

- Beam Xing << detector response times (few nsec vs 100-1000ns)



Very Clean Events

e+e+ vs $p\bar{p}$ Environment



Aleph $Z \rightarrow \mu^+\mu^-$ Event
Only 2 Tracks

CDF $Z \rightarrow \mu^+\mu^-$ Event
Many Tracks over 500MeV/c

Signatures for $p\bar{p}$ Triggering

Accept specific decays modes

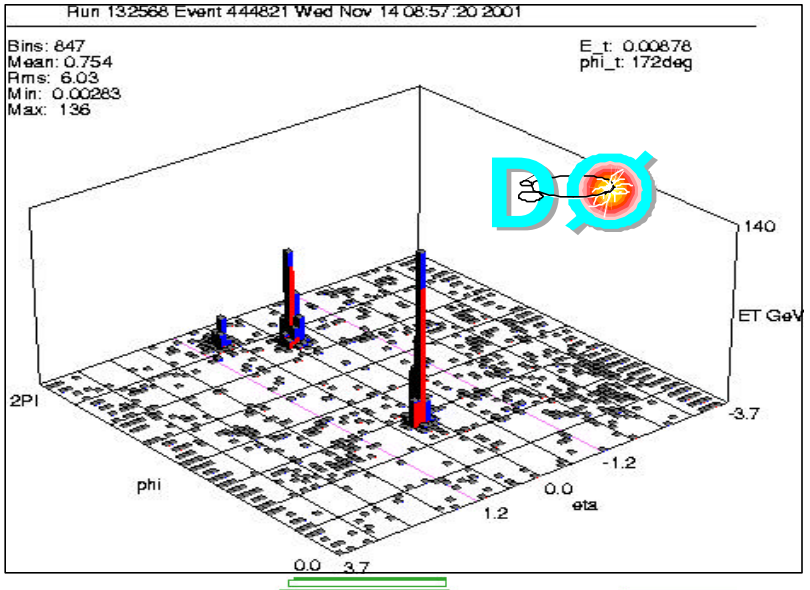
- High P_T leptons from W, Z, top, W/Z+Higgs QCD: High Et jets
- $\Upsilon \rightarrow \mu\mu$, medium pt leptons for B physics

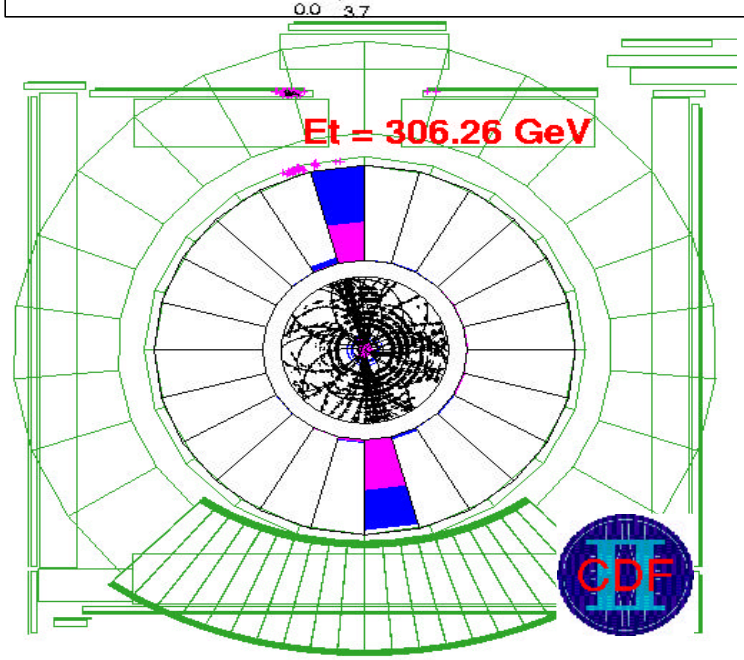
Reject:

- Lower P_T objects (QCD)

Select on object/event kinematics:

- E_T of in Calor Tower (cluster), missing E_T
- μ P_T (+ track P_T)
- Track P_T (+ impact parameter/detached vertex)





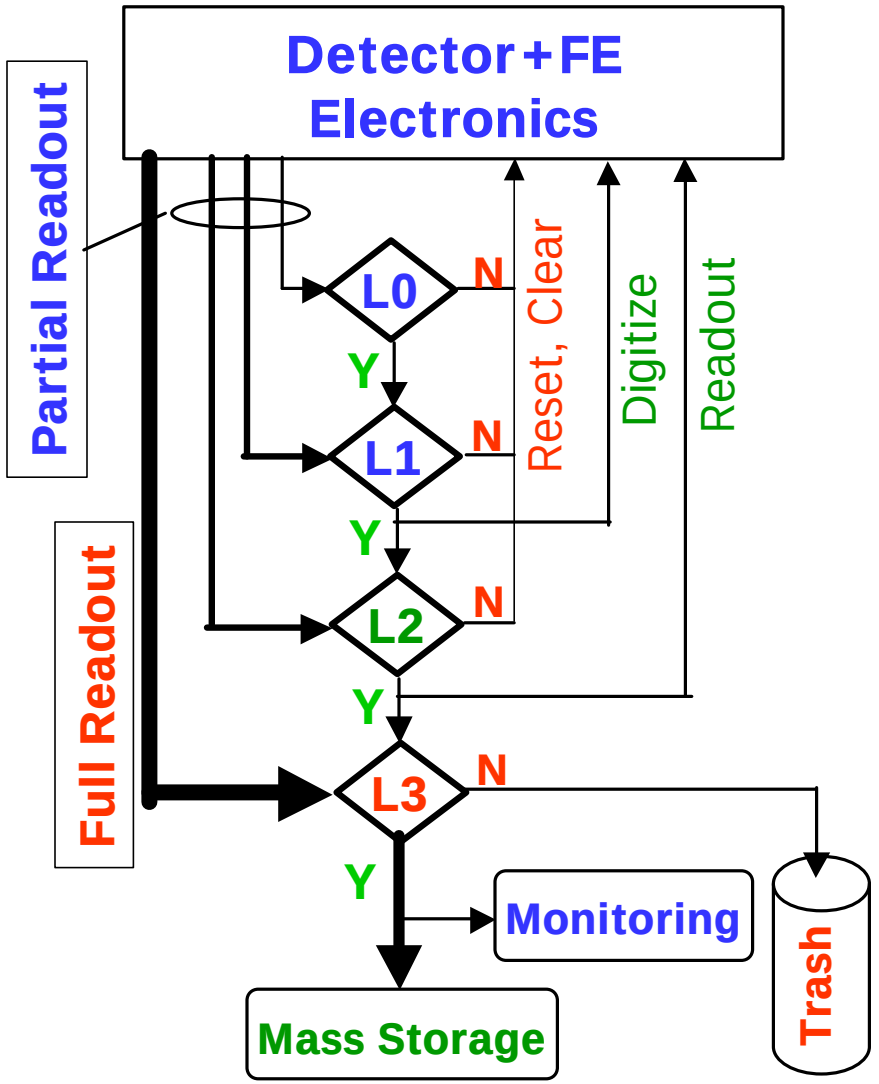
Multilevel Trigger Systems

Multi-Level Trigger Systems

High Effic ⟺ Large Rejection

- Can't achieve necessary rejection in a single triggering stage
- Reject in steps with successively more complete information
  - L0 – very fast (<~bunch x-ing), very simple, usually scint. (TOF or Lumin Counters)

    Few expts use a L0 anymore
  - L1 – fast (~few μs) with limited information, hardware
  - L2 – moderately fast (~10s of μs), hardware and sometimes software
  - L3 – Commercial processor(s)



Example: D0 Run 1 (1991-95)

L0 Trigger (285kHz in, 150kHz out)

- Beam hodoscopes

L1 Trigger (200Hz out)

- Single Cal trigger towers (4 thresh)
- Global E_T and missing E_T (EM, HAD)
- Muon chamber tracks
- No deadtime, exec. time <1 μs

L1.5(2) Trigger (100Hz out)

- Higher resolution muon chamber tracks
- TRD confirmation for electrons
- Execution time: up to 100μs

L2(3) Trigger (2Hz out)

- Farm of Vaxes running offline type code

D0 Trigger and DAQ System

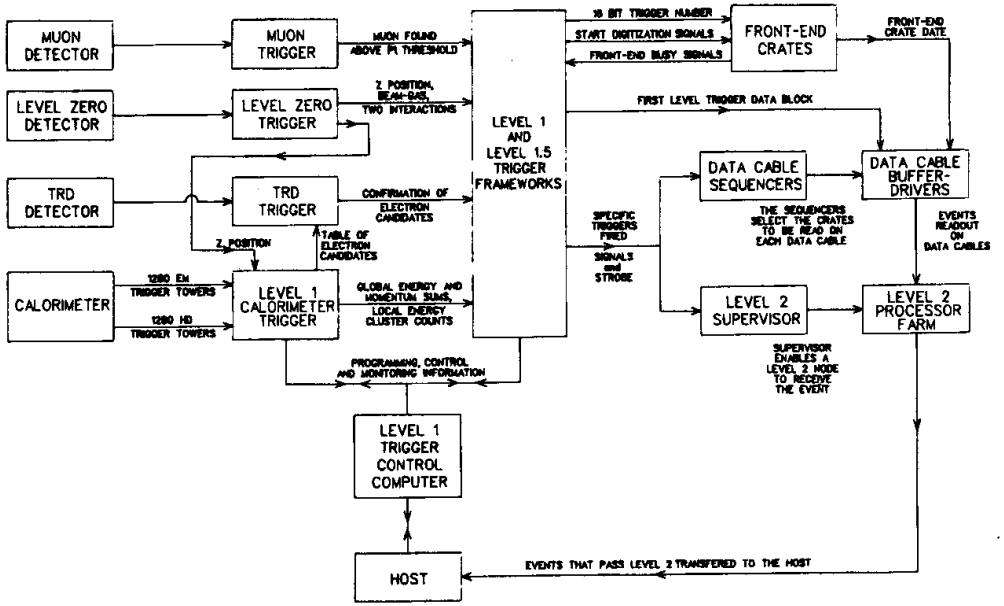


Fig. 67. Block diagram of the trigger and data acquisition system.

S. Abachi et al NIM A338 (1994) 185.

Example: CDF Run 1 (1988-95)

Every 3.5ms (bunch spacing):

- Calorimeter Sample and Hold get reset
- Muon and CTC TDC get stop

L1 Trigger (285kHz in, 1.5kHz out)

- Trigger decision on fast output of Beam-Beam, Calorimeter, and Muon
- Execution <3.5μs ⇨ no dead-time

L1 Accept ⇨ stop gating detector

L1 Reject ⇨ continue gating detector

L2 Trigger (up to 50Hz out)

- Add CTC tracks and match to muon and Calorimeter clusters
- Execution 30-50μs ⇨ dead-time <10%

L1 Accept ⇨ digitize and readout

L1 Reject ⇨ resume gating detector

L3 Trigger (up to 5-8Hz out)

- Event size 300kB in, 100kB out
- Farm of SGIs running offline type code
- Readout ~3ms, Readout deadtime <10%

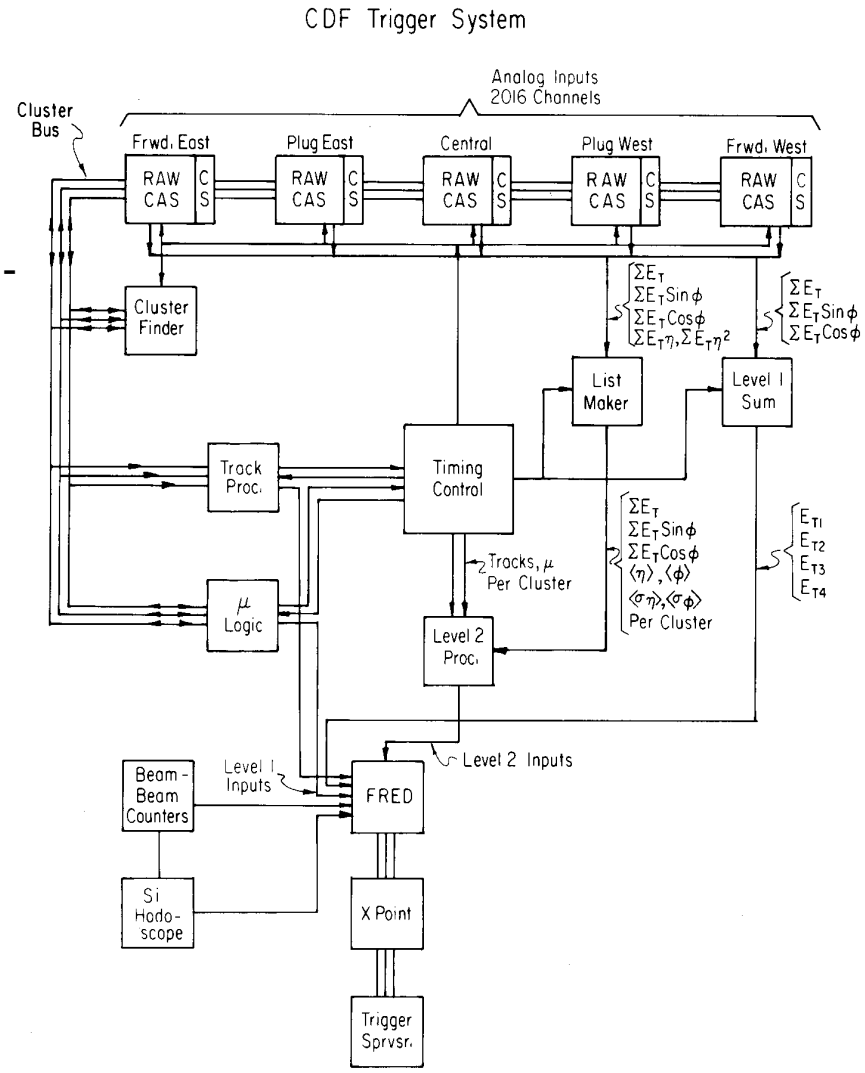


Fig. 1. A block diagram of the CDF Level 1 and Level 2 trigger system.

D Amidei et al NIM A269 (1988) 51.

CDF/D0 Run 1 Implementations

CDF

- Fastbus: ~20 designs, ~20 crates in counting rooms
- Calorimeter Trigger
  - 0.2x0.2 Tower $\eta-\phi$ – analog sum and sin θ weight
  - Sample and hold (>50μs), DACs and comparators for thresholds (2)
  - ΣE_T and Missing E_T: analog Σ, FADC, digital Σ
  - ~3μs L1 execution
  - L2 analog/digital clustering (contiguous towers)
- Muon Trigger
  - Time difference in pairs of layers (two Pt thresholds)
  - Scintillator and Hadron Cal confirmation
- Global L1 Decision (in RAM)
  - 12 Inputs, 16 outputs
  - Counts of muon stubs by region, Cal tower, no ϕ info

D0

- VME (9U): crates in moving and fixed counting houses
- Calorimeter Trigger:
  - 0.2x0.2 Tower $\eta-\phi$ –analog sum and sin θ weight
  - FADC on sum, digital threshold (4)
  - ΣE_T and Missing E_T: RAM and digital sum (z-vertex correct)
  - Pipelined <1μs execution
- Muon Trigger
  - 3 layer patterns of hits
  - Apply Pt threshold for L2
- Global L1 Decision (and-or network)
  - Up to 256 inputs, 32 outputs
  - Counts of towers, muons above threshold by region
  - If L2 confirmation required wait for L2

CDF/D0 Run 1 Implementation

CDF L2

- Drift Chamber Tracks
  - Digital pipeline finds tracks serially scanning 360^{o} in ϕ
  - Eight PT bins from
  - Track P_T, ϕ_0 feed Cal and Muon matching hardware (15^{o}, 5^{o} match respectively)
  - Fast CMOS rams and AS TTL logic
- Other: Fine grain shower max info for electrons and Calorimeter Isolation trigger using analog NN chip
- Programmable processors (custom Fastbus) apply final event cuts:
  - 1A: Motorola bit slice
  - 1B: DEC Alpha
- Up to 64 different L2 triggers possible
- Other than track processor almost completely based on ECL logic

D0 L2

- No drift chamber tracking (no solenoid)
- 16 muon bits from finer matching
- L2 Triggers pre-requisite on L1 triggers
- Uses same global decision (L1 Framework) logic as L1

Example: CLEO II Trigger (ca 1989)

TOF (Cal) trigger (L0,L1,L2):

- discriminators on each bar (Σ 16 X-tals) and OR'd into 30(32) sectors
- >1 sector, 2 opposite, non-adjacent

BLT, TSP triggers (L1,L2):

- Count low P_T tracks (threshold algorithm) and determine charge (BLT)

PD trigger (L2):

- Vertex chamber path consistent with coming from beam spot

Hadron Trigger

L0 TOF non-adjacent

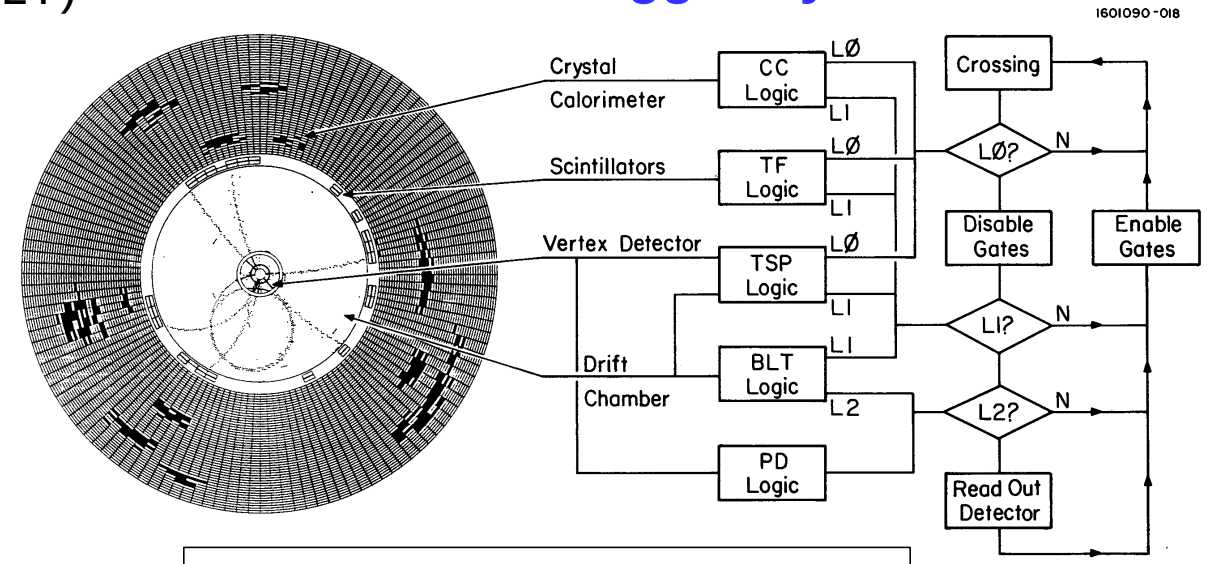
L1 Three tracks

L2 Two PD tracks

Continuously gating sample and holds

Stage	Devices Used	Output	Execution Time	Dead Time
L0	Cal, TOF, VD	20kHz	<360ns	0
L1	Cal, DR, TOF, VD	20Hz	2.56ms	5%
L2	Cal, DR, VD	5Hz	50ms	0.10%
ReadOut	N.A.	5Hz	12ms	1.20%

CLEO Trigger System



C. Bebek et al NIM A302 (1991) 261

Pipelined Trigger Systems

Pipelined Trigger & FE: Zeus, H1

Large proton-beam background:

- $\sigma_{pp} \gg \sigma_{ep}$
- bad vacuum (synchrotron radiation)

bunch crossing rate: 10.41 MHz (96ns)

⇒ Pipeline trigger

beam-gas rate: ~ 100 kHz (10000ns)

- Can't make decision in 1 step

⇒ Three-Level Trigger

L1 (FLT) : Hardware triggers

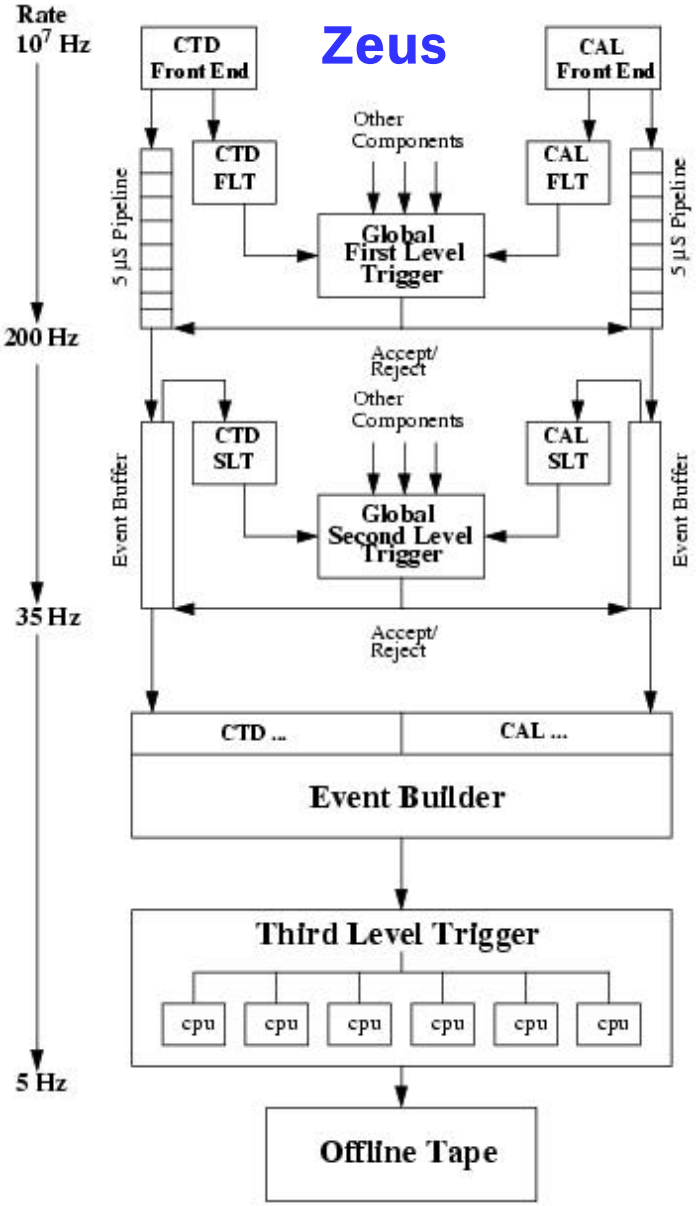
starts readout (digitization)

L2 (SLT): Software trigger with distributed processors

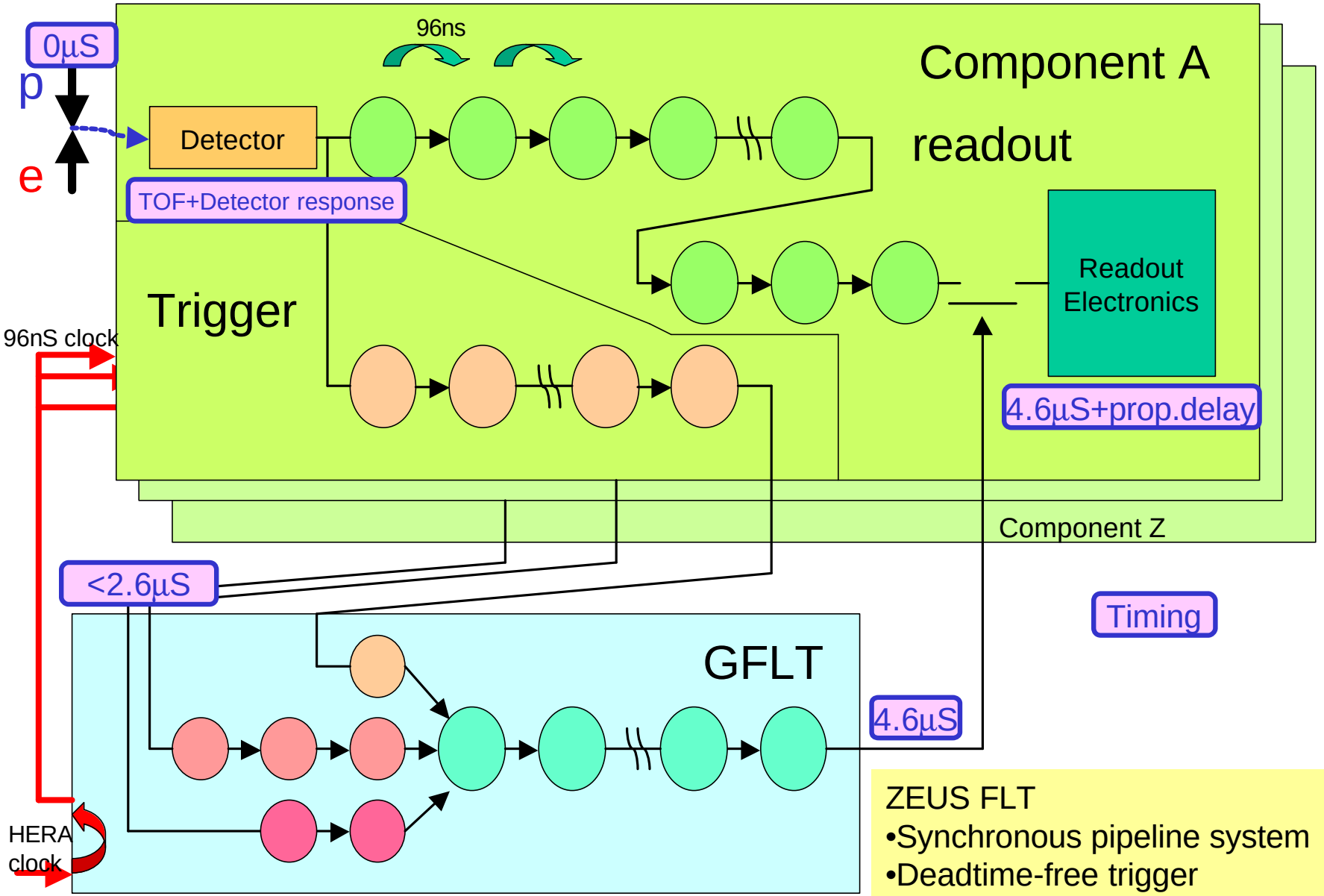
starts event building

L3 (TLT): Software trigger in a single processor

starts data storage



Pipelined Trigger Operation: Zeus



Rejecting Beam-Gas at Zeus and H1

Primary task is rejecting Beam-Gas background:

- Timing of TOF hits (H1) rejects out of time events
- Track processors reject events with large impact parameter in r-ϕ and r-z planes to remove beam-wall and beam-gas backgrounds
- Example: Look for patterns in r/z across layers:
  - Good tracks constant r/z
  - Tracks not from interaction region will have wrong pattern

Zeus Track Z0 Finding

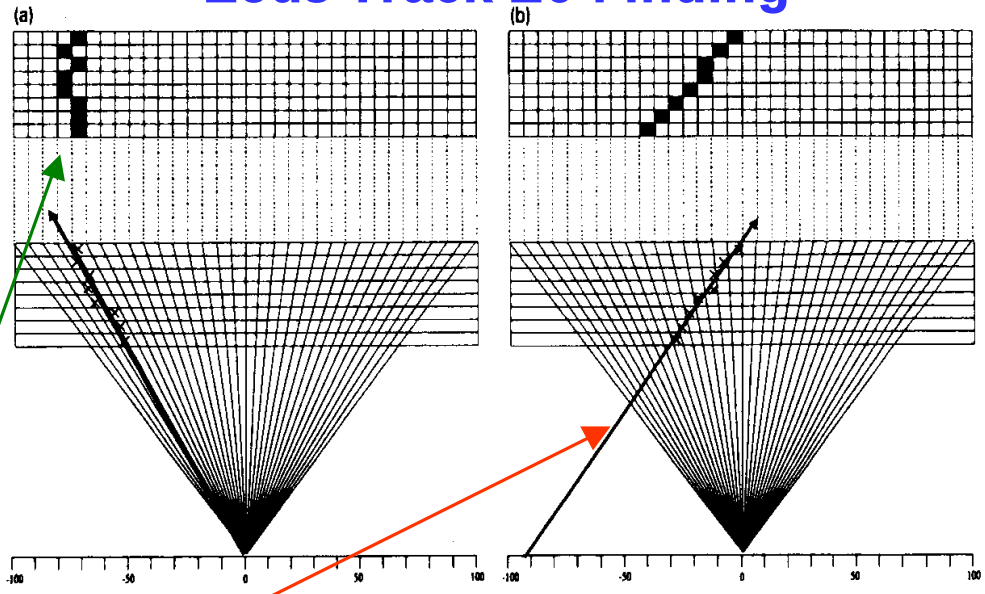


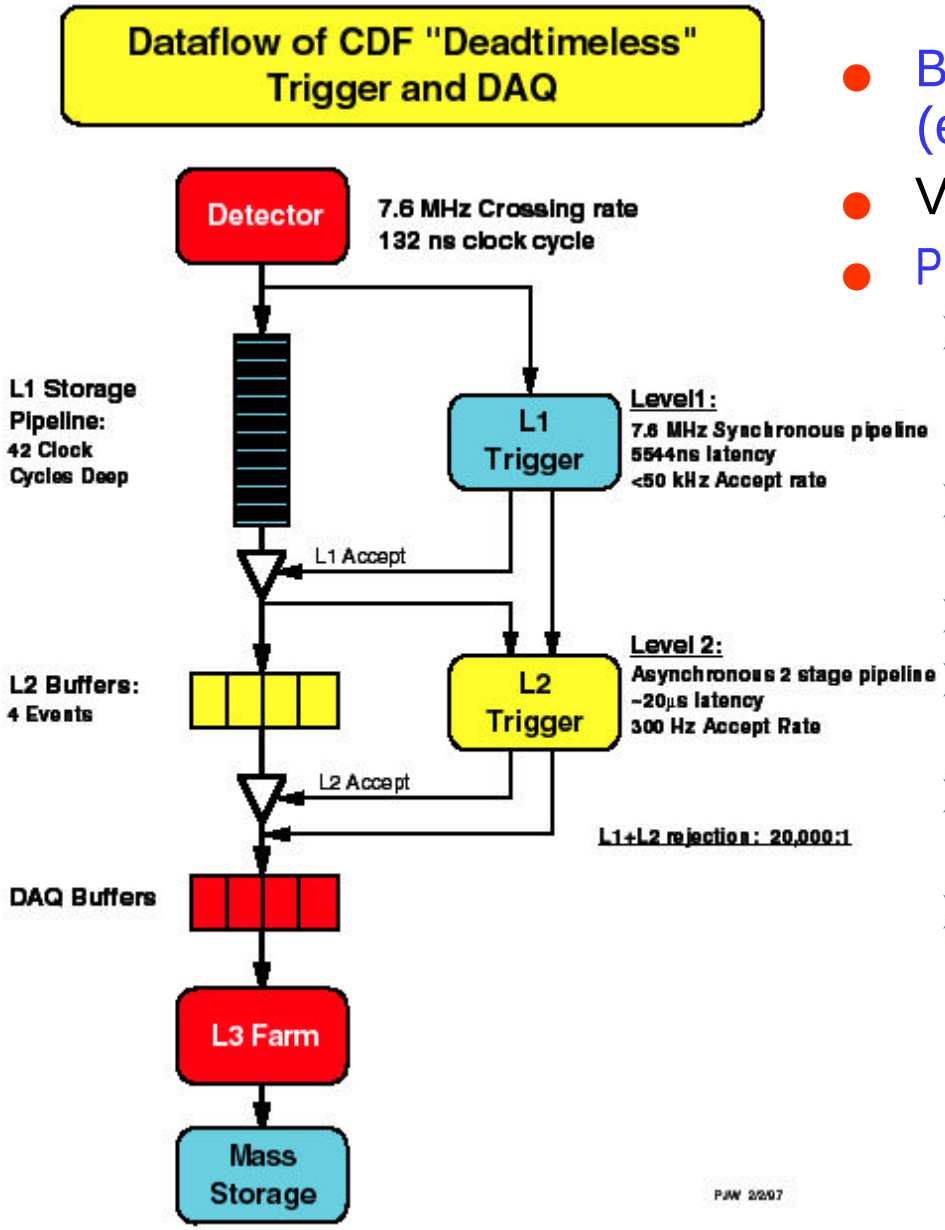
Fig. 2. The formation of the z/r table in the segment finding processor for (a) a track from the vertex region and (b) a track from outside the vertex region.

GP Heath etal, NIMA 315(1992) 431.

Also can be effective for beam backgrounds at e+e- machines

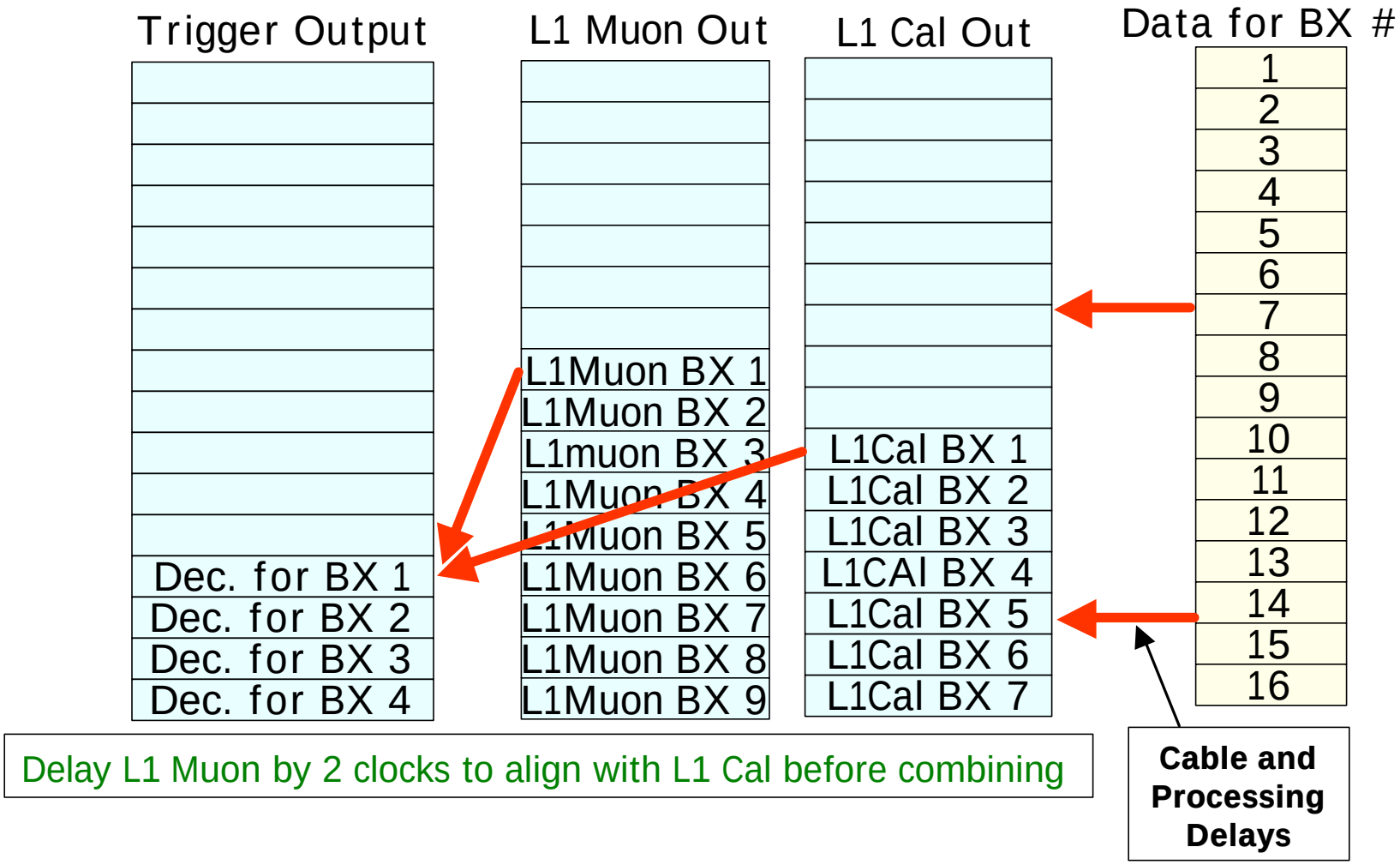
(OPAL, M. Arignon etal NIM A313 (1992) 103.)

CDF/D0 Pipelined Trigger/DAQ



- Beam x-ing always multiple of 132ns (either 132 or 396)
- Very similar to Zeus design
- Pipelined DAQ+Trigger:
  - Every front-end system stores data for at least 42 clock cycles during L1 decision
  - All L1 trigger processing in parallel pipelined operation
  - L1 decision is made every 132 nsec
  - On L1 accept, data is moved from L1 Pipeline and stored in L2 buffers
  - On L1 reject data is dropped off end of pipeline
  - On L2 accept data is read into VME Readout Buffer (VRB) modules awaiting readout via switch to L3

Getting Pipelines in Synch



Need to design in time alignment wherever comes together

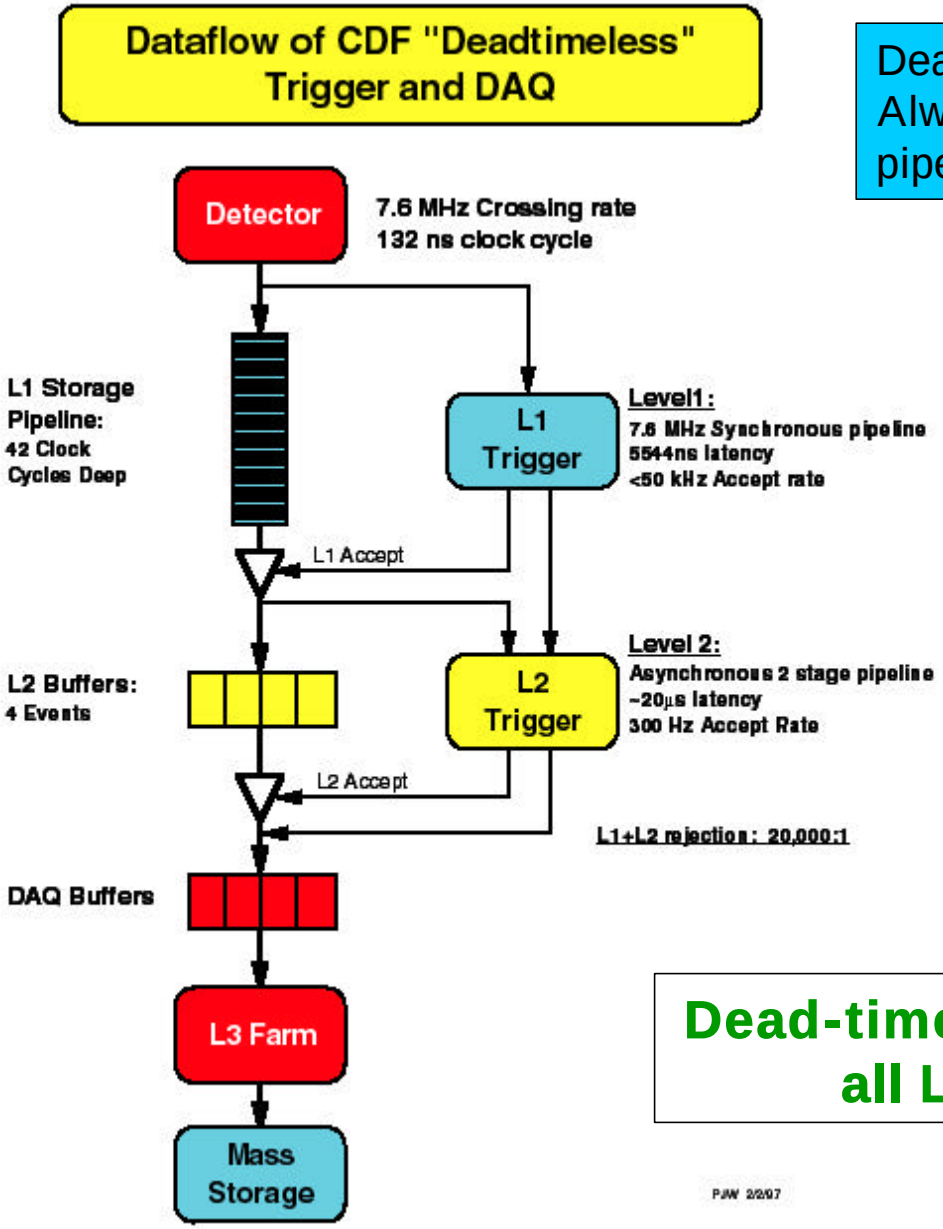
Keeping Pipelines in Synch: Bx Counters

- Critical for pipeline system design to provide method(s) of determining if pipelines are staying in Synch
- Common method: bunch x-ing counters in each component or passed which reset once per accel turn
  - Count fundamental clock even for unfilled buckets
  - CDF and D0: count 7.6MHz (132ns) clocks (0-158), actual number of beam x-ing per accelerator turn is 36 (104) for 396ns (132ns) accelerator operation (its actually a clock counter).
  - Distribute to each component: fundamental clock and beginning of turn marker, called bunch 0 (b0) at Tevatron

Staying in Synch: Bunch X-ing Checks

- CDF: bunch counter readout from each board into event data
  - Compare between boards in VME readout controller (PowerPC SBC). Out of synch pull local error line.
  - Compare between crates at event building time. Out of synch send error message
  - Can miss occasional short term synch problems
  - Most frequent problem: errors in bunch counter logic on board
- Zeus passes BX number along with data in L1 pipe to test synch at decision time
  - Some CDF components pass B0 mark: test every 21μs

Dead-time in Pipelined Trigger



Dead-time cannot be incurred by L1 Trigger. Always complete before data comes off end of pipeline. L1 Deadtime ➡ Broken System

L2 incurs Dead-time if all L2 buffers fill up before completing L2 decision. L1A must be held off.

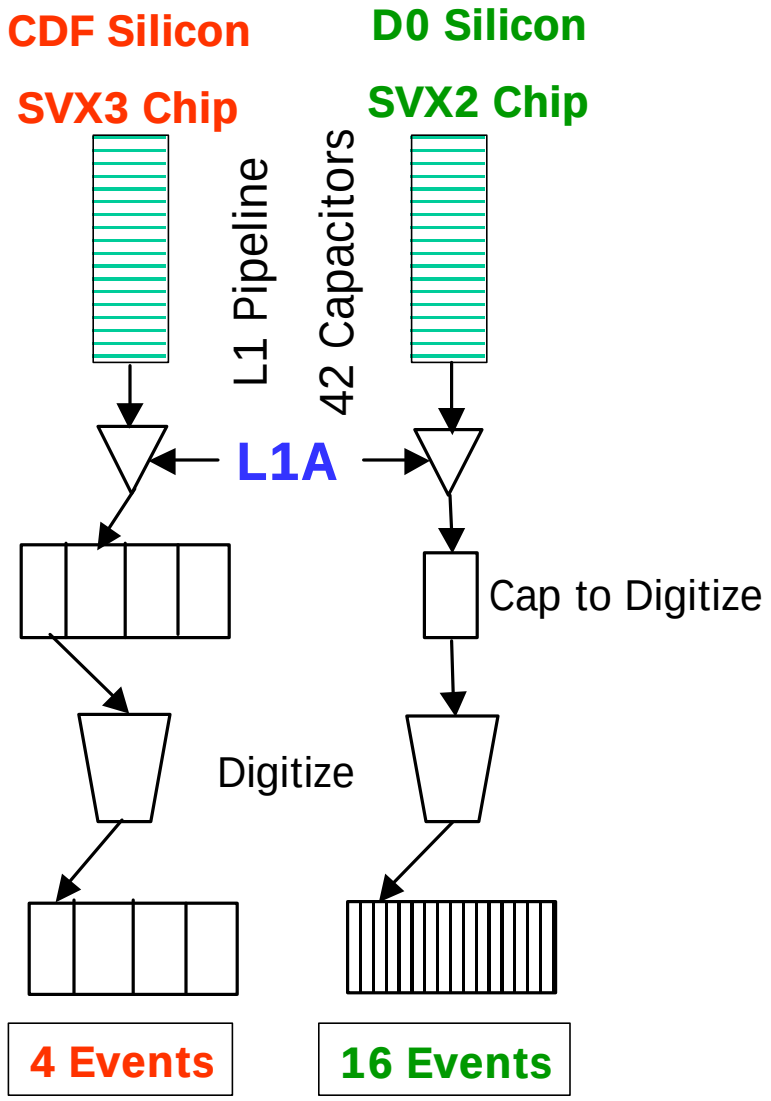
Read-out incurs Dead-time if VRB buffers fill up ➡ then L2 buffers will fill and L1A must be held off.

L3 incurs deadtime if the switch has no node to send output to. Again system backs up until L1A is stopped..

Dead-time is only incurred when all L2 buffers are full

CDF/D0 Si Readout effects Trigger Design

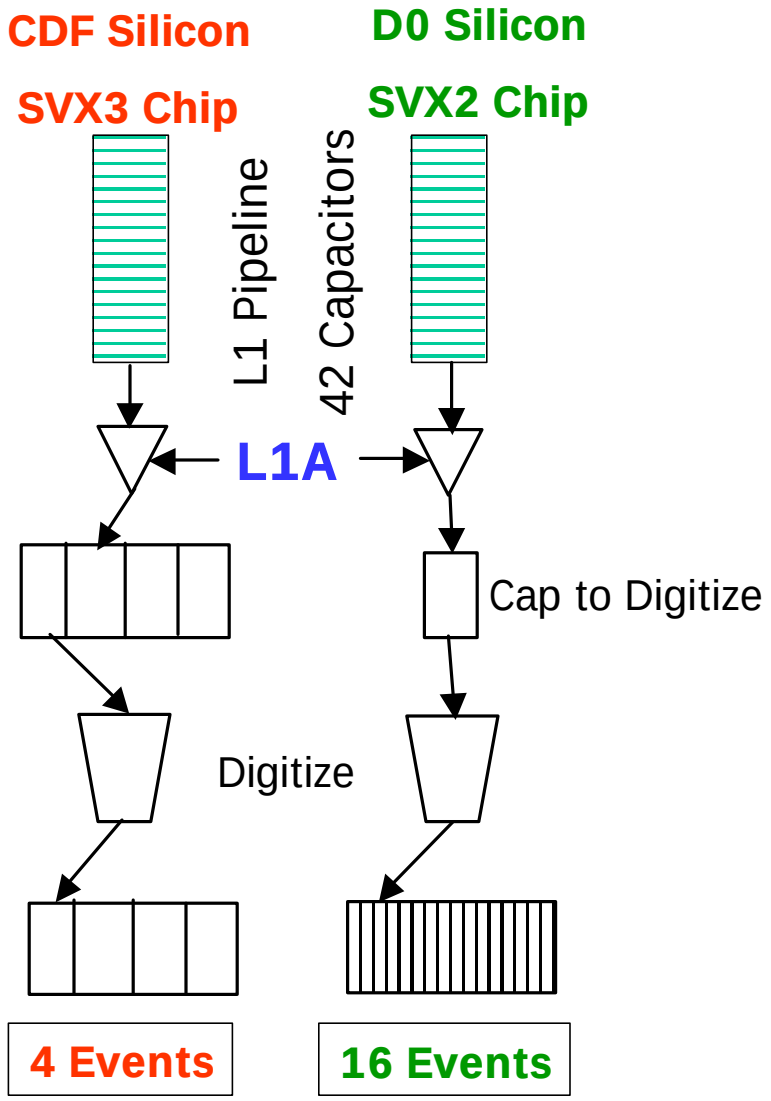
- L1 pipelines implemented many ways: capacitor array, RAM, shift register (eg in FPGA), discrete FIFO
- L2 buffering also implemented many ways: capacitor array, RAM, discrete buffer chips
- CDF and D0 Si strip detectors use a capacitor array for the L1 pipeline and digitize on L1A
  - Capacitors are controlled as circular buffer.
  - 128 Channels on digitized sequentially
  - CDF uses SVX3 chip: has 4 additional capacitors and skip logic that permit additional L1As during readout
  - D0 uses SVX2 chip: dead during digitization and readout (~10μs).



L2 Buffer on VME Readout Buffer

Impact of Si Readout on CDF Trigger

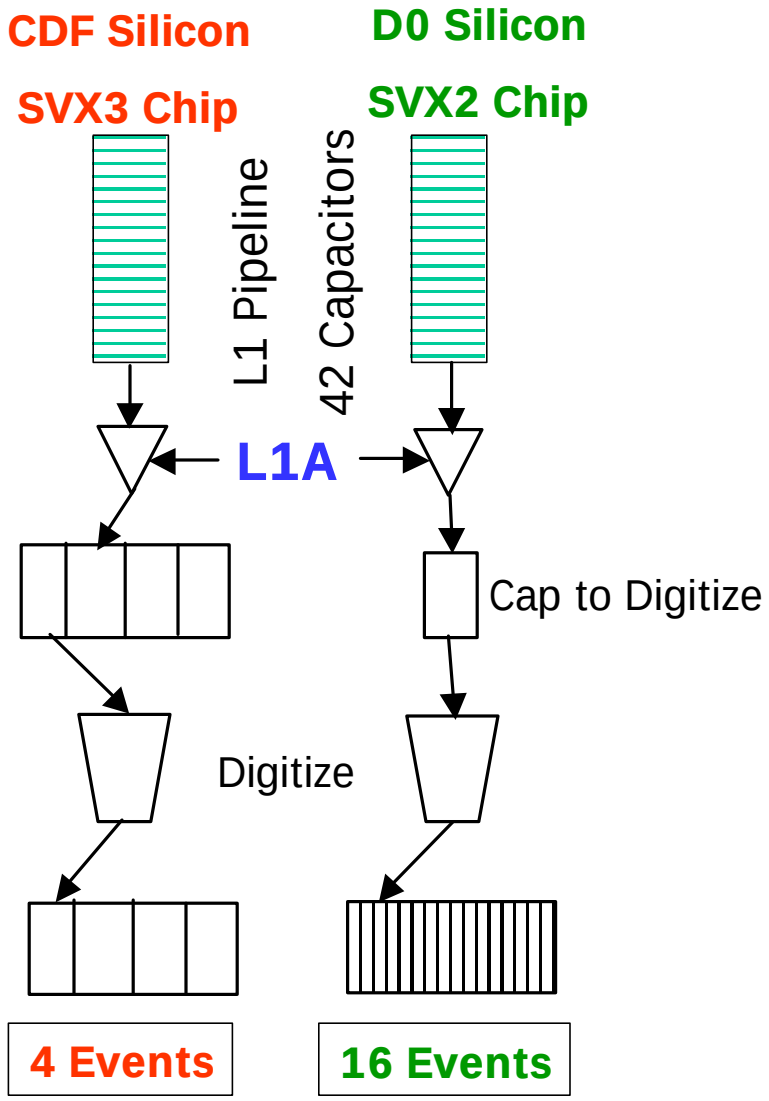
- All CDF frontends are designed with 4 L2 buffers like SVX3 chip. All others are digitized before L1 pipe
  - Could not put additional capacitors on SVX3 die
  - Hard to put more buffers on TDC ASIC for drift chamber (JMC96 from U.Mich)
  - Queuing simulations showed system could operate with low ~5% deadtime at L1A=45kHz if L2 execution kept <20μs in two stage pipeline
  - Little benefit from pushing for more L2 buffering in VME Readout Board (VRB)
  - ➔ Design high rate L1 trigger (45kHz) (B→hadrons)
  - ➔ Design fast L2 processing (~20μs)



L2 Buffer on VRB Board

Impact of Si Readout on D0 Trigger

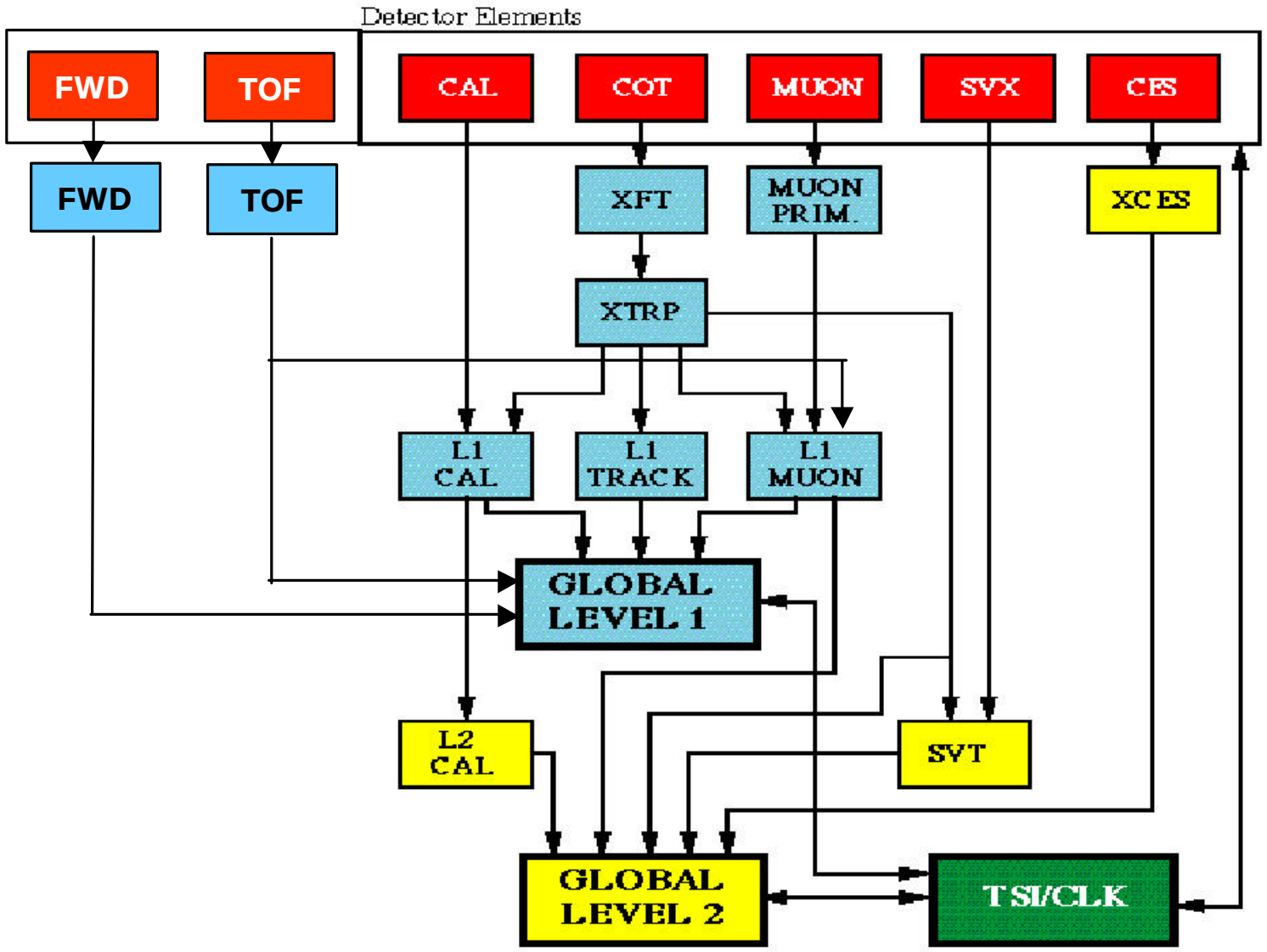
- Since D0 has SVX2 chip for Silicon and Fiber tracker readout, detector is dead for ~10ms after L1A
  - ➔ Limit L1A to ~5-10kHz
  - ➔ Queuing simulations show benefit from more VRB buffering
  - ➔ With low L1 rate and more buffering, can take more time for L2 processing ~100μs
  - ➔ See later how this impacts L2 design



L2 Buffer on VRB Board

Components of Modern Trigger Systems

CDF Trigger Subsystems



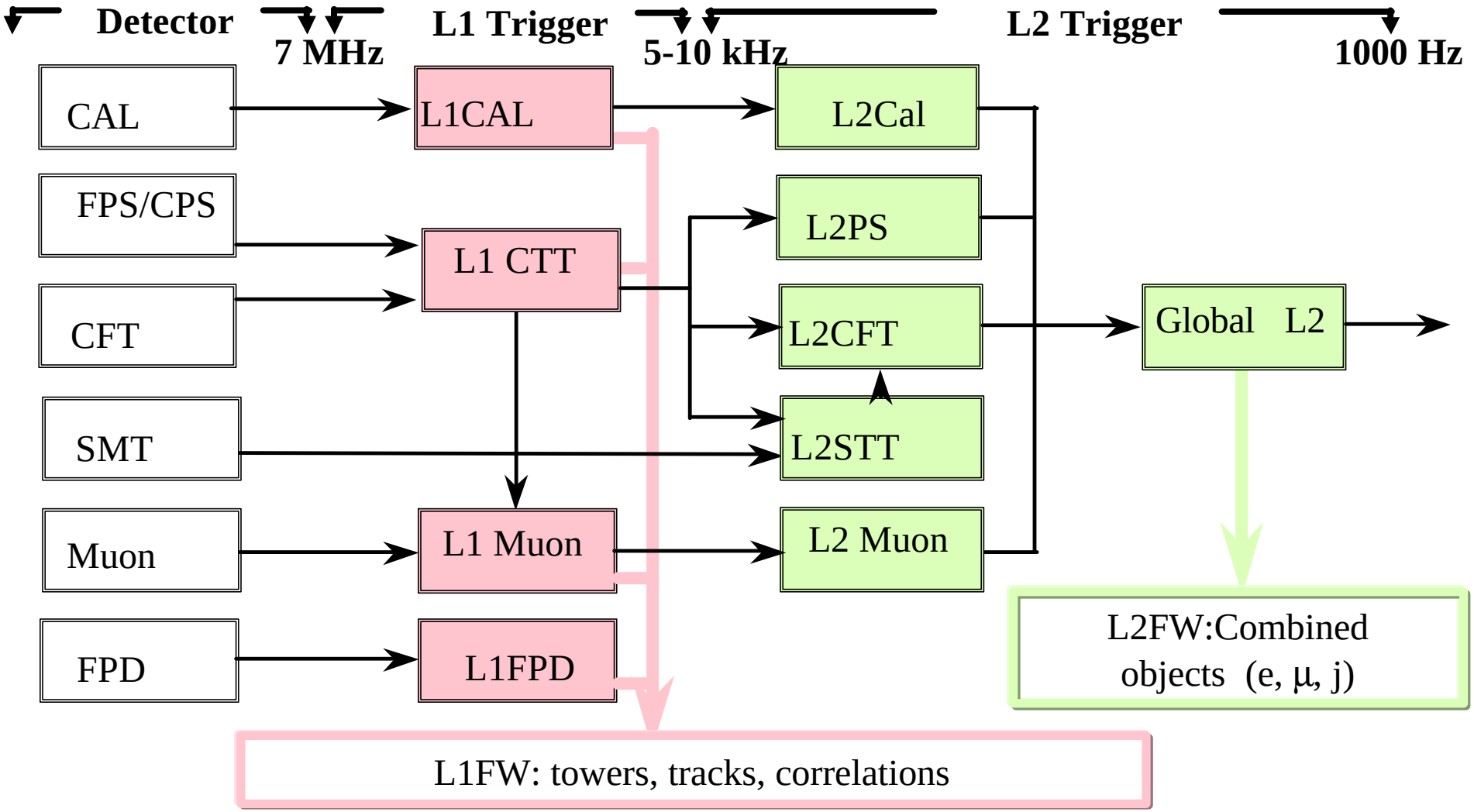
FE – 66 9U VME Crates

L1 – 15 9U VME Crates

L2 – 15 9U VME Crates

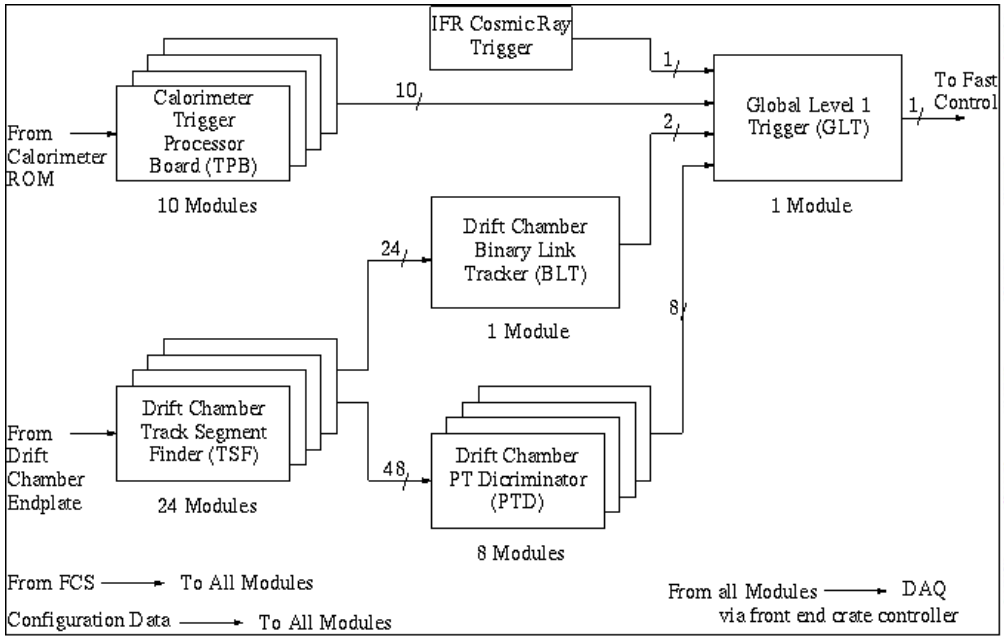
Trigger Supervisor 3 9U VME Crates

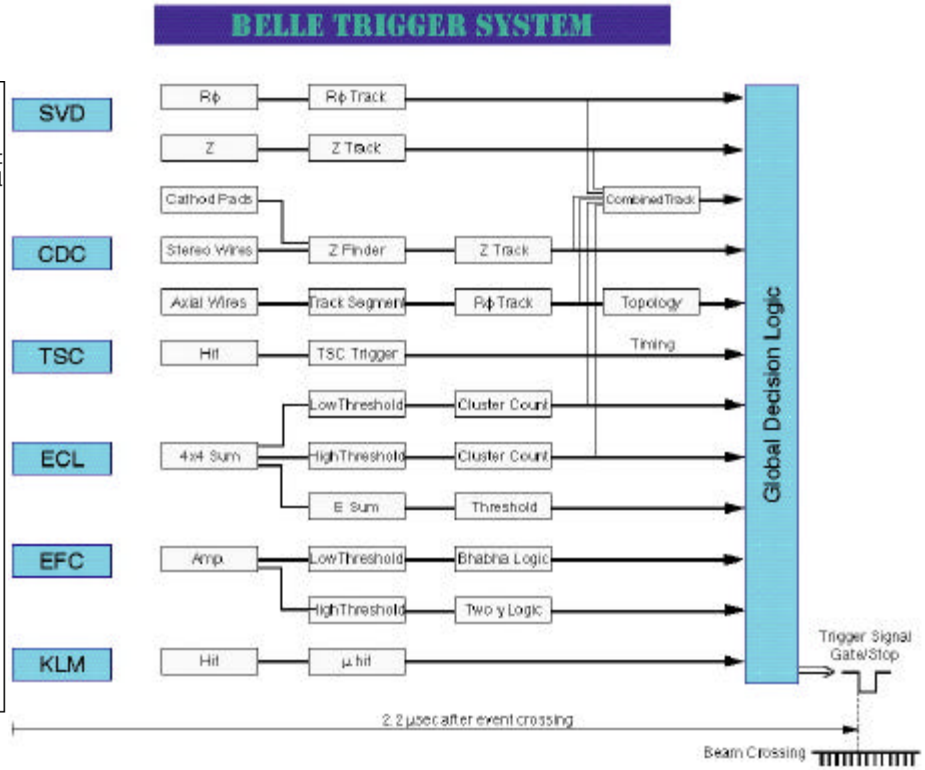
D0 Trigger Block Diagram



L1 Trigger Systems: Belle and Babar

Babar L1 Trigger





Similar approaches... similar performance

No L2 Triggers

L1 Trigger Strategy

- Select objects: muon, electron (photon), jet, track by applying threshold cuts in subsystem processors (custom hardware)
  - Tevatron – fine granularity and lots of E_T/P_T thresholds for different physics (eg top vs B's)
  - B-Factories , LEP – coarse granularity few thresholds
  - Hera – combination of above
- Track finding difference
  - Tevatron ➔ Cut on P_T, god resolution and many bins
  - B-Factories, LEP and HERA ➔ Number and ϕ correlation of tracks above minimal P_T, z information to reject beam background
- Two strategies for combining objects:
  - CDF (and D0 muon) ➔ fine Track match in subsystems, pass global count to decision logic. Complex subsystem logic, Simpler final decision logic
  - B-Factories, LEP and HERA ➔ Send counts in coarse geometric regions to global and do correlations there. Simpler subsystem logic, more complicated final decision

Comparison of L1 Trigger Systems

	CDF	D0	Babar	Belle	Zeus
L1 In (MHz)	7.6	7.6	<<238	<<125	10.4
L1 Out (kHz)	45	10-May	2	2	1
Latency (μs)	5.5	4.2	12	2.2	5
Clock (MHz)	7.6 (30.4)	7.6	14.8/30.6/?	16/32/64	10.4
Tracking	r-φ (48 PT Bins)	r-φ (20 PT Bins)	r-φ	r-φ, r-z	r-φ, r-z
Track dP_T/P_T^2	1.5%, <1% w/Si	1-1.5% w/Si	3 Threshold	2 Threshold	2 Threshold
Muon	μ stub&track	μ stub&track	Track, MIP	Track, MIP	MIP&ISO
Calorimeter Seg.	0.2x0.2 (η - φ)	0.2x0.2 (η - φ)	18° φ wedge	4x4 or 17 θ bins	896 Tower
Photon	E_T&HAD/EM	E_T& PreShow	E	E	E&ISO
Electron	E_T&HAD/EM&Track	E_T& PreShow&Track	E, Track	E, Track	E&ISO
Jet	Total E_T	E_T (Tile)	NA	NA	NA
Global Energy	ΣE_T, Missing E_T	ΣE_T, Missing E_T	E	E	E, ΣET, Missing ET
TOF	MIP, HIP	N/A	N/A	MIP Coinc	N/A
Forward (Diff)	Yes	Yes	N/A	N/A	N/A
Decision: Input bits	64	256	138	48	314
Decision: Triggers	64	128	24	48	64
Decision Logic	Two stage: X-Point + Ram	Multistage: AND-OR	Two Stage: φ corel RAM, RAM	RAM	Multilayer RAM

L1 Framework/Global Decision Logic

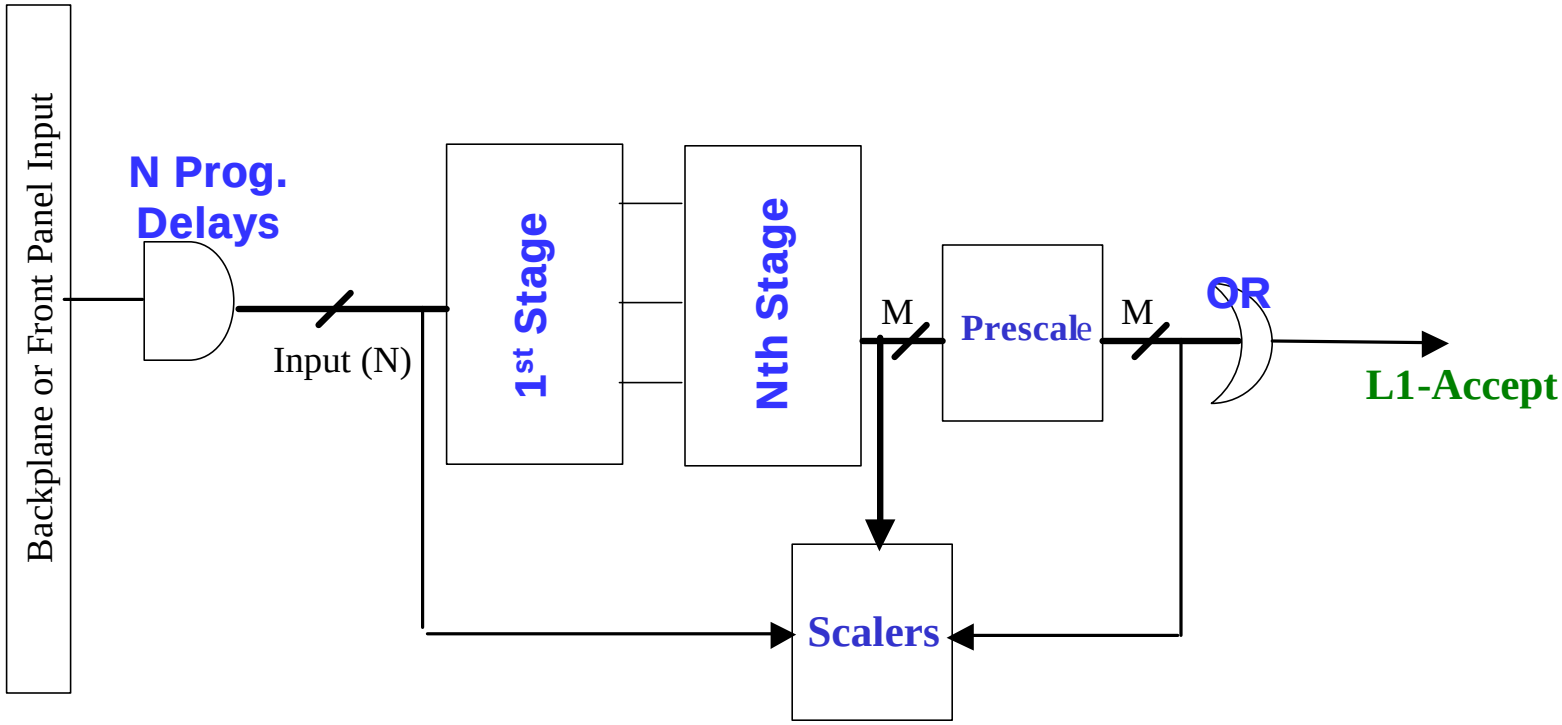
Decision logic typically implemented in RAM very flexible in allowed combinations

Combinations limited by software to configure the RAM

Can be arranged in several stages to allow more flexible combination

Prescale counters used for monitoring trigger

Scalers are used to count both in puts and outputs



CDF/D0 L2 Trigger Strategy

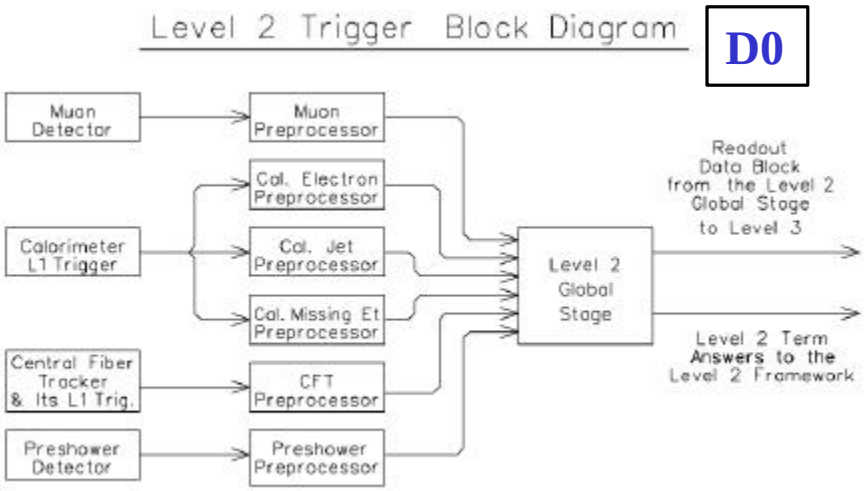
Two stage process:

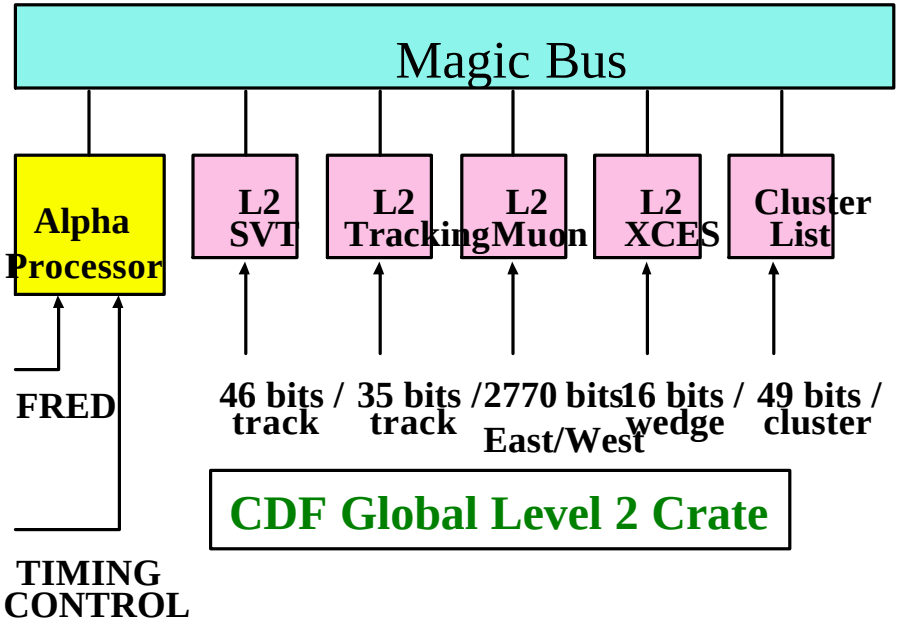
1. Reconstruct objects: muon, electron/photon, jet, tracks in pre-processors and pass object kinematics to central processing
   - Some input information will be the same as used at L1 (e.g. tracks from central tracker)
   - Remaining information will be newly formed (e.g. Silicon tracks with impact parameter measurement)
2. Assemble event in processor memory and run event filters much like a L3 trigger except on a very limited scale
   - Processor is custom VME module based on DEC Alpha chip
   - Filters written C/C++ and run

CDF/D0 L2 Triggering

Same architecture and Processor but different implementation

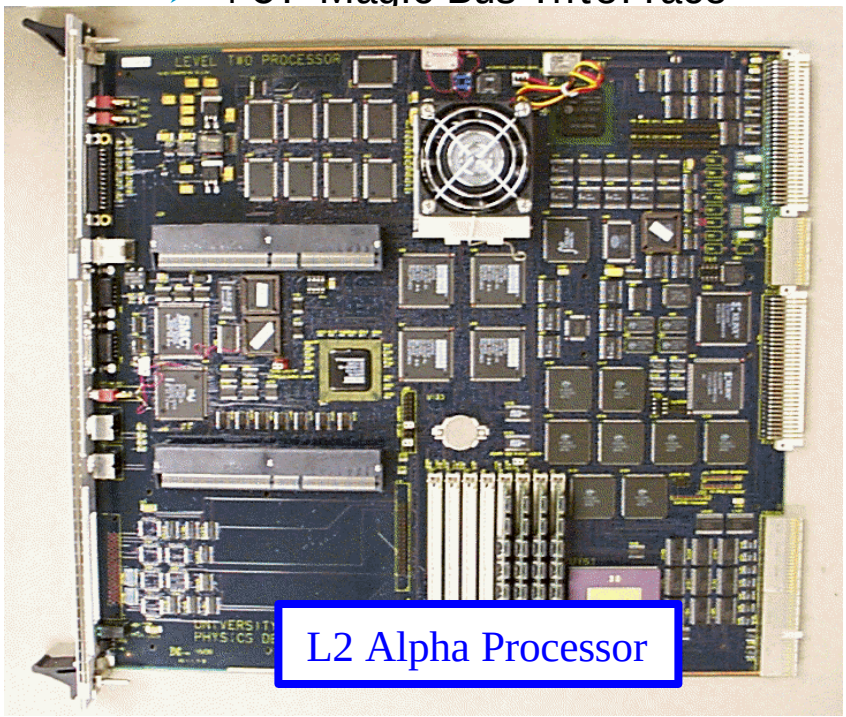
	D0	CDF
Execution (design)	100μs	(10+10)μs
SiTracker	Hardware	Hardware
Other PreProcesors	DSP+Alpha	Hardware
Decision Proc	Alpha	Alpha
OS	Linux	Native





Level 2 Alpha Processor

- Custom MagicBus – 128bit wide on P3 for Trigger I/O
- Processor is based on DEC Alpha PC164 board design
- Three custom circuits
  - PCI-VME Interface
  - Magic Bus DMA input
  - PCI-Magic Bus Interface



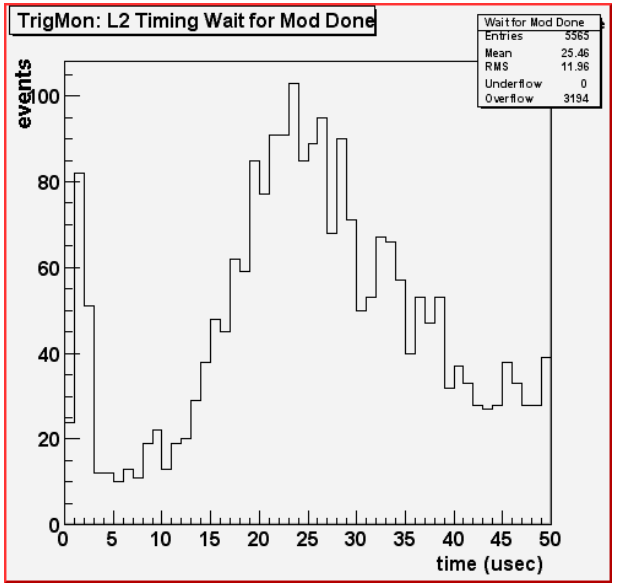
- Very low PCB yield
  - Via's failed after bed of nails test due to incorrect manufacture
  - Ok for CDF near term (need 1-4 + spares)
  - Bad for D0 need >20
  - Many Parts obsolete
- Replace with new design as Run 2B upgrade:
  - D0 Beta – commercial PCI SBC on custom adapter (PCI-VME and PCI-MagicBus). Prototyping complete.
  - CDF L2 Pulsar – new generic L2 interface with S-link output to LINUX-PC. Prototype being tested

CDF L2 Trigger Performance

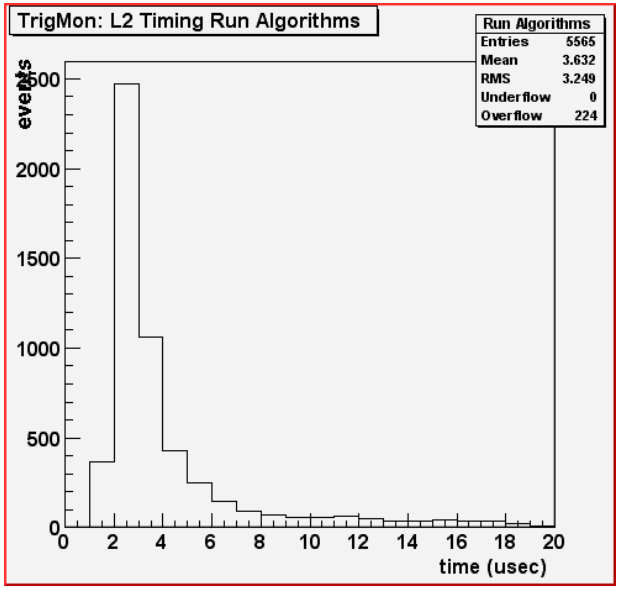
CDF L2 designed as 2 stage pipeline (10-15μs/stage)

- L1 Bandwidth closely tied to performance of this pipeline
- First stage loading limited by Si Readout + SVT execution (currently 9μs+13μs=22μs)
- Algorithm time is much faster than first stage but has long tails
- Total Si Readout limited at 25μs (L00 readout). Need to keep this less than total of 2 stages.
- It doesn't matter yet because: L1A rate currently limit set at 12kHz due to SVX chip wirebond failures

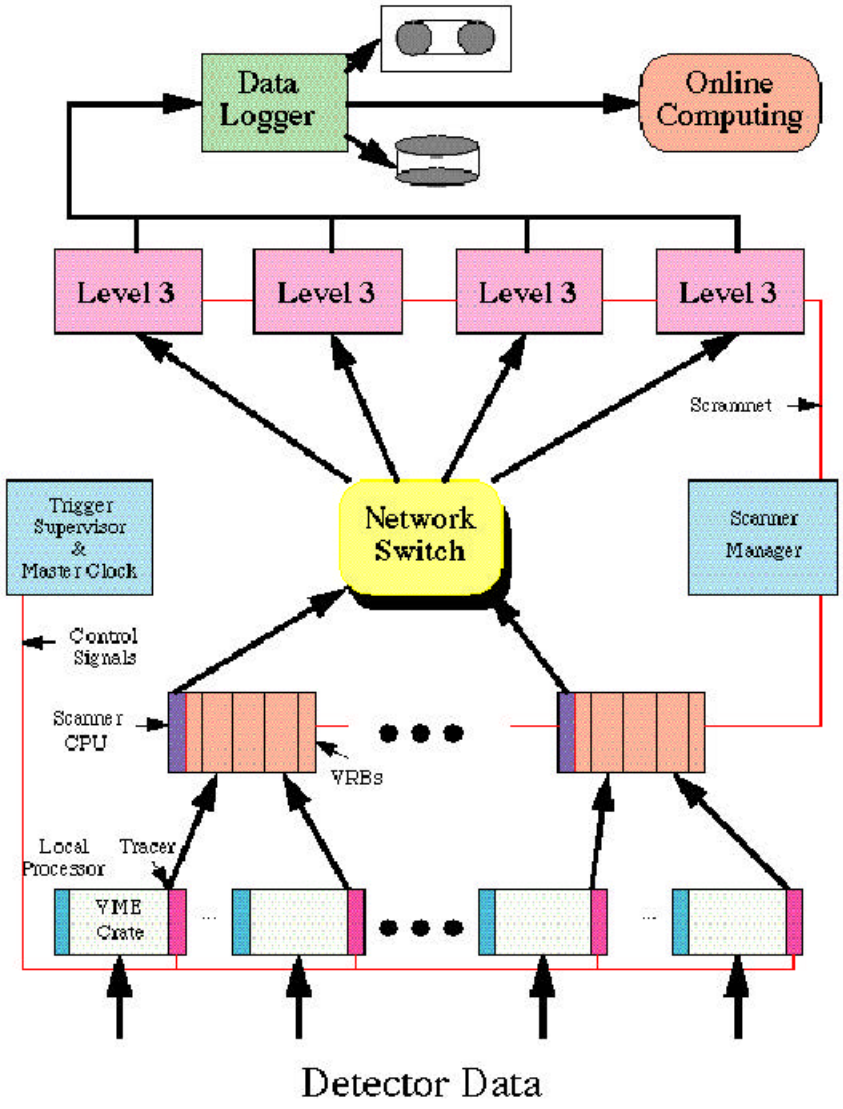
Loading



Algorithms



CDF/D0 DAQ and L3 Systems



- Mostly commercial hardware (switch, links etc)
- Custom VME Readout Buffer
  - G-Link or Taxi input available
- Custom interfaces to L1/L2 triggers
  - CDF Trigger Supervisor
  - D0 contained in Trigger Framework
- L3 runs off-line based algorithms

	D0	CDF
VME FE Crates	300	110
VRB Crates	20	15
Switch	Gb Ethernet	ATM
L3 -Linux	80 dual	250 dual

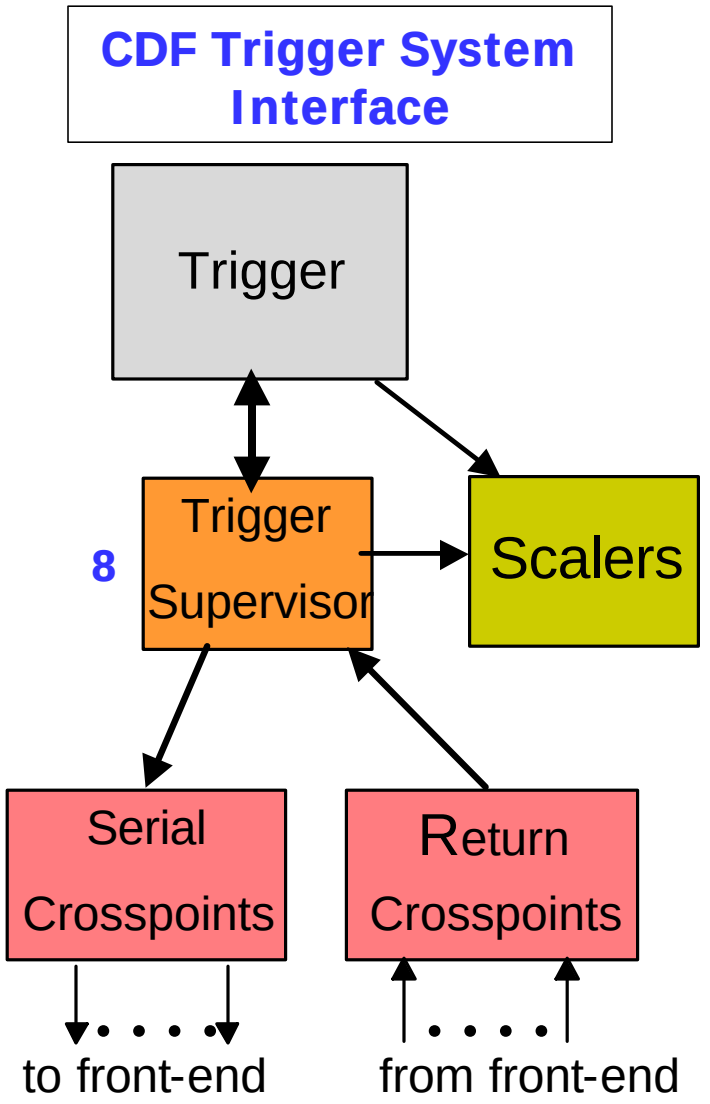
Trigger Managers/Supervisors

Trigger decision hardware determines if event should be stored need to determine if it can be (eg full buffers)

⇨ Trigger Supervisor (CDF)

⇨ Part of Trigger Framework (D0)

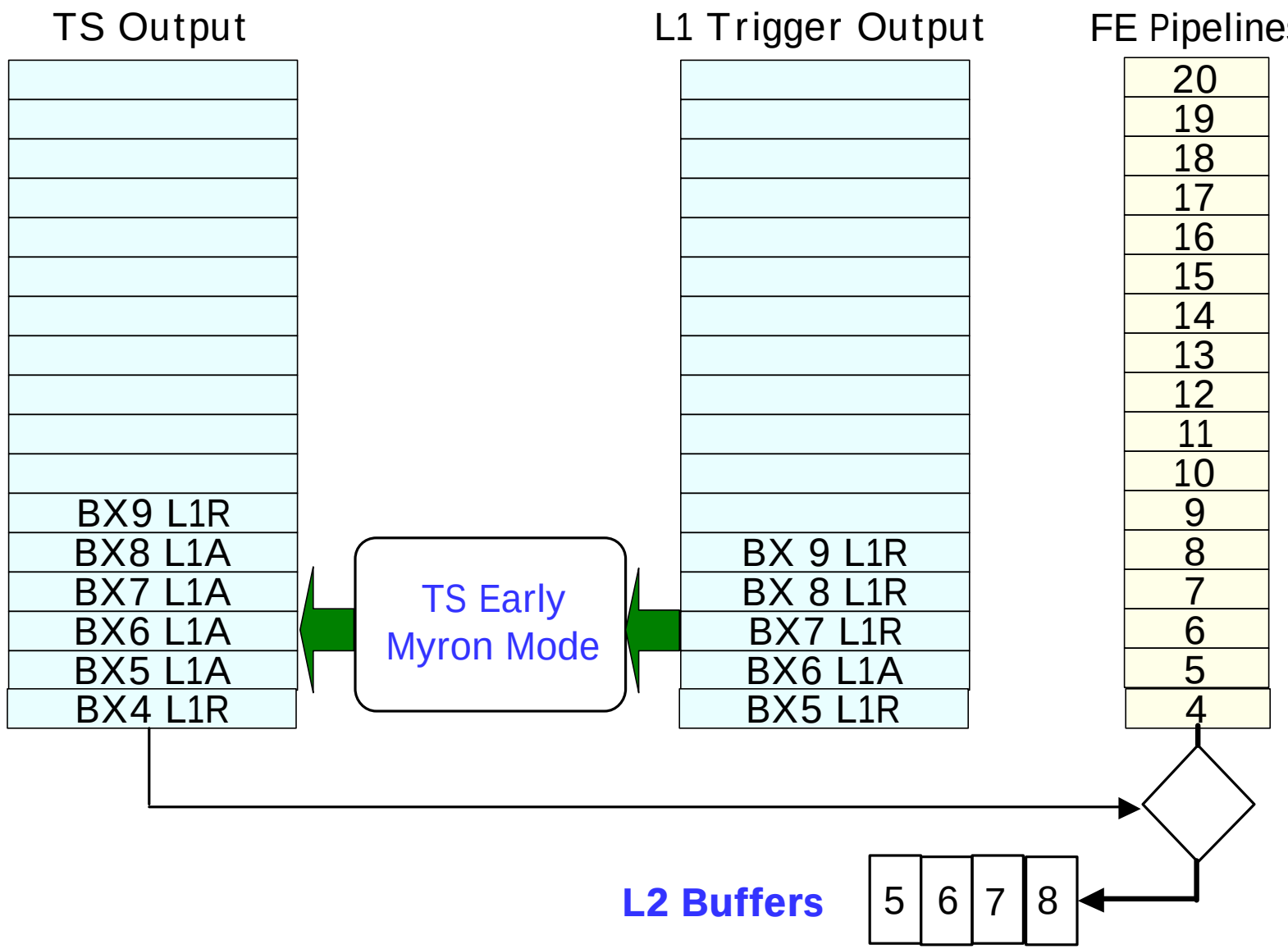
- Distribute commands to and receive acknowledges from front-end and trigger crates
  - L1 and L2 Accept/Reject
  - L2 Buffer assignments (CDF)
  - Start scan (readout)
  - Event ID (L2 only at CDF)
  - Read list number (up to 8 different ones)
  - Done
  - Busy
  - Error
- Manage L2 buffer assignment (CDF)
  - Different L1 Pipeline and L2 buffers implementations, one control interface
- Manage and measure live/dead time
- Count Triggers in Scalers



System Features for Debugging

- Multi-partitioning
  - Parallel independent DAQ systems (8 at CDF)
  - At CDF only one partition with real trigger
  - At D0 can have specific triggers for Geographic sections
- Internally generated triggers
  - Bunch 0 (CDF)
  - Arbitrary bunch 0-158 (D0)
- CDF "Myron" Mode (after Myron Campbell)
  - Use L2 buffers on all systems as shallow (4 deep) logic analyzer with up to 750K input channels
  - One L1A from Trigger results in L1A from TS for 4 successive clock cycles (system dead from L1A to completion of readout)
  - Two start points: triggered clock or previous clock ("Early Myron Mode")
  - Only makes sense with L2 in auto-accept mode
  - Very useful for timing detector elements with each other both horizontally and vertically in decision chain

CDF Pipeline as Big Logic Analyzer



Supporting Software

- Triggers configured from a list of requirements (“Table”, “List”…). Determine thresholds, logic of L1 Decision hardware, L2 software loaded
  - Kept in a database for tracking
  - Software must interpret and convert into down load information
- For verification and monitoring, data is read out from locations along trigger decision path. Used in monitoring code to verify correct operation in comparison to an emulation of algorithms.
- Online monitoring
  - Rates of trigger decisions and inputs
  - Run emulation on subset of events
  - Look at occupancy distributions for objects

Hardware Implementation Development

Trigger Hardware Progress

- Need to condense a large number of signals to a final in a short time
- Premium on fast, high density processing, preferably re-programmable
  - c 1980 – ECL (high power dissipation)
  - c 1990 – RAM, Shift registers, PALs, small CPLDs, gate arrays, multiple layers for complicated tasks
  - c 2000 – CPLDs, FPGAs, large RAM, FPGAs with embedded RAM ASICs see less use than in FE due to high initial cost
- Analog ➔ Digital triggers:
  - 1988 CDF Cal trigger – analog summing, discriminators
    - Digitize after accept, hard to confirm trigger decision offline
  - 1990-92 D0, Zeus initial analog sum, digitize then final sum and thresholds
    - Readout of trigger data used for decision
  - 2000 CDF uses same digitized input for readout and Trigger in Calorimeter and Silicon (D0 too with Silicon)

CDF/D0 Upgrade Implementations

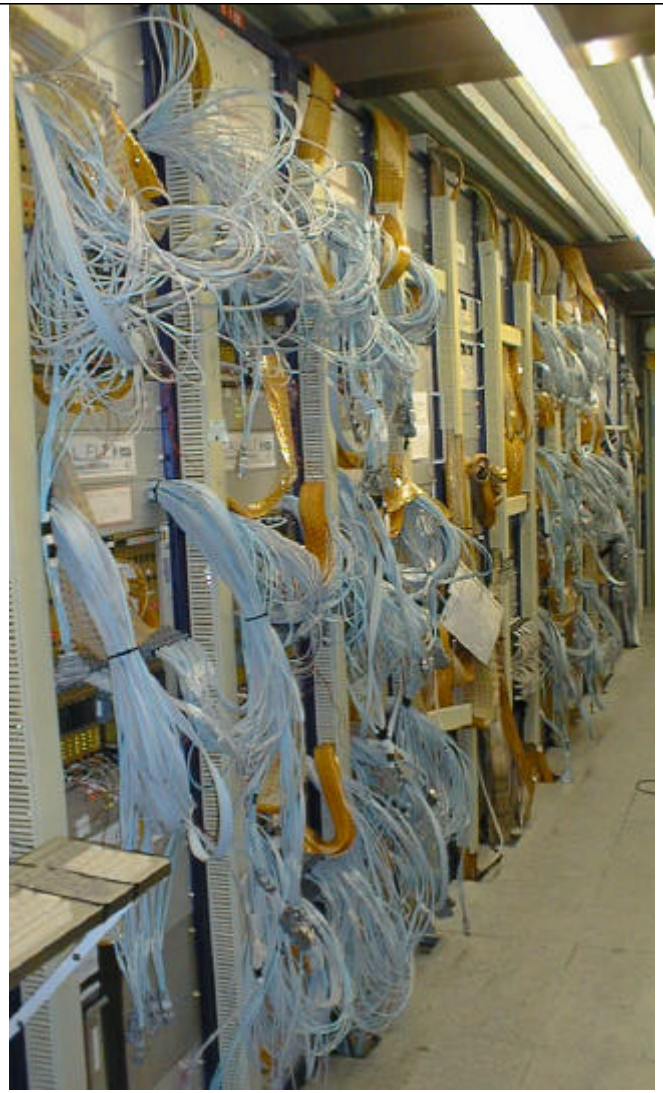
- While ASICs are abundantly in use for Front-end readout they are only used in a limited way in our triggers
  - CDF SVT Associative memory (INFN Pisa), could done in FPGA now (see Giovanni this afternoon)?
  - CDF Data-phasing chip (U. Michigan), could easily do in small FPGA of CPLD
  - D0 none?
- Extensive use of XILINX and Altera FPGAs
  - CDF L1 Calorimeter trigger could now be built on much smaller boards (designed ~95-96)
- New designs can be very flexible: CDF L2 Pulsar card
  - Pattern generator for L2 test stand
  - Planned to be centerpiece of L2 upgrade
- Boards that were most easily integrated at CDF were the ones with lots of test features such as ways to load and readback diagnostic data (e.g. SVT has circular buffer at input and output of each board.

Trigger Hardware – 9U

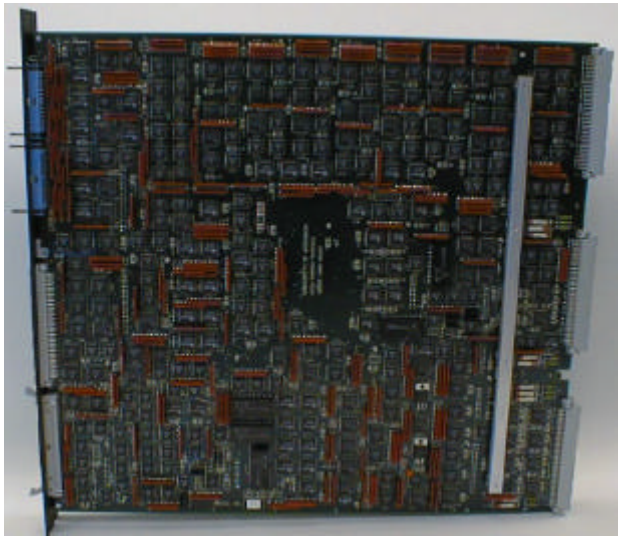
- Choice of 9U VME: Lots of board space for logic
  - Large amount of front panel space for I/O
  - Transition (Aux) card space for additional I/O

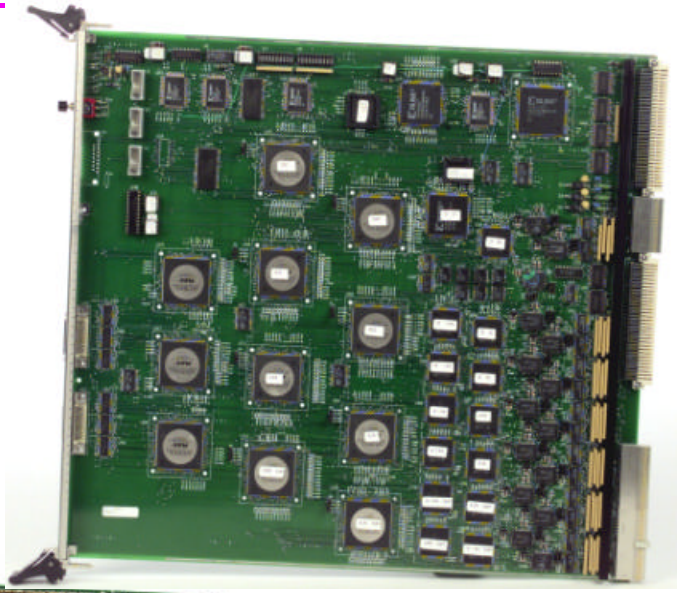
CDF L1&L2 Calorimeter Triggers: 12 9U Crates

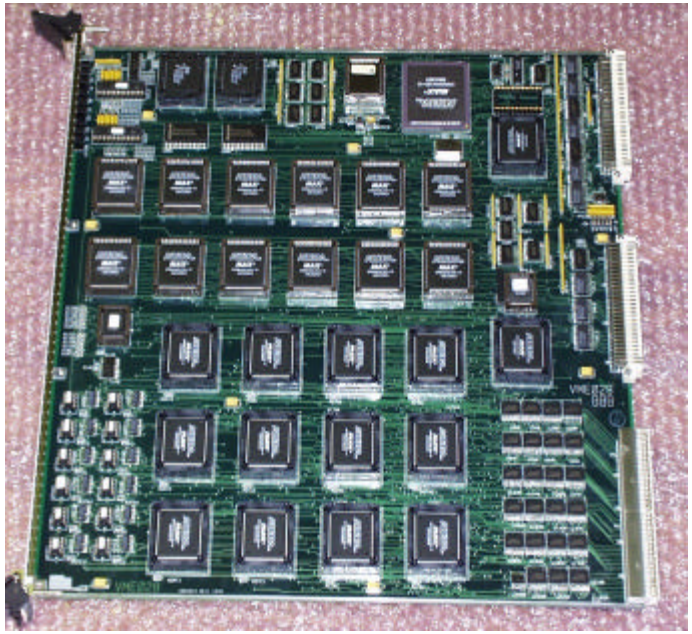
Zeus Calorimeter Trigger: 16 9U Crates

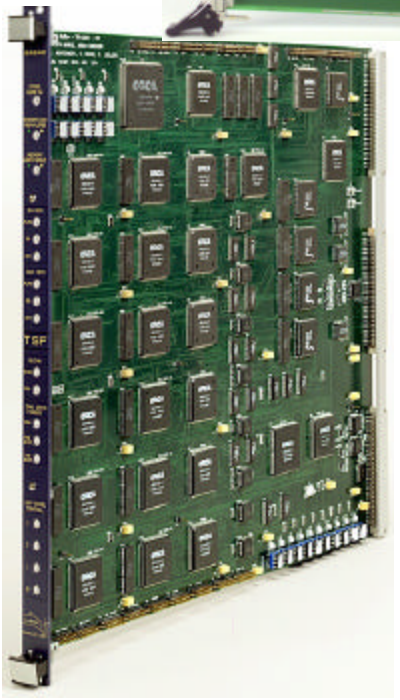


Deep Down they are all the same!



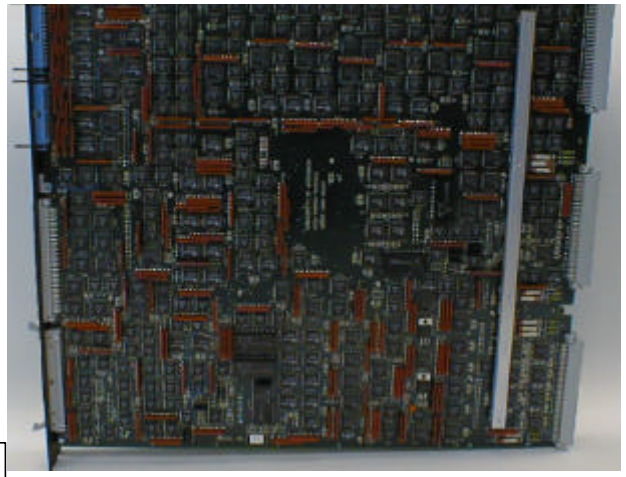




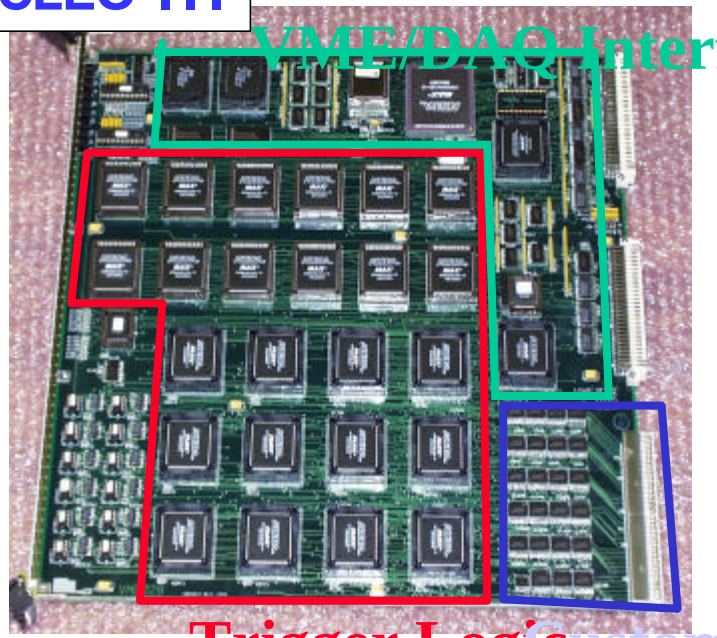


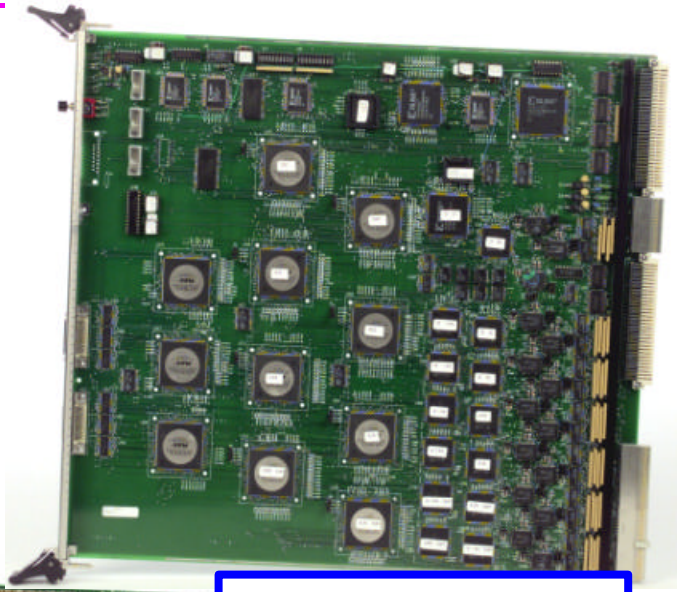
Or maybe not?

Zeus Calorimeter Trigger Adder Card

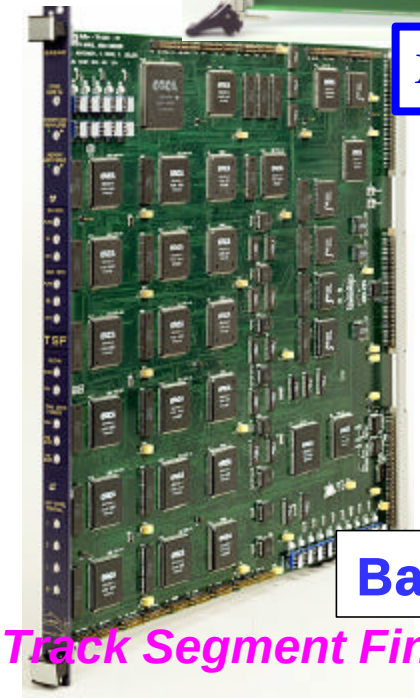


CLEO III





XFT FINDER - CDF

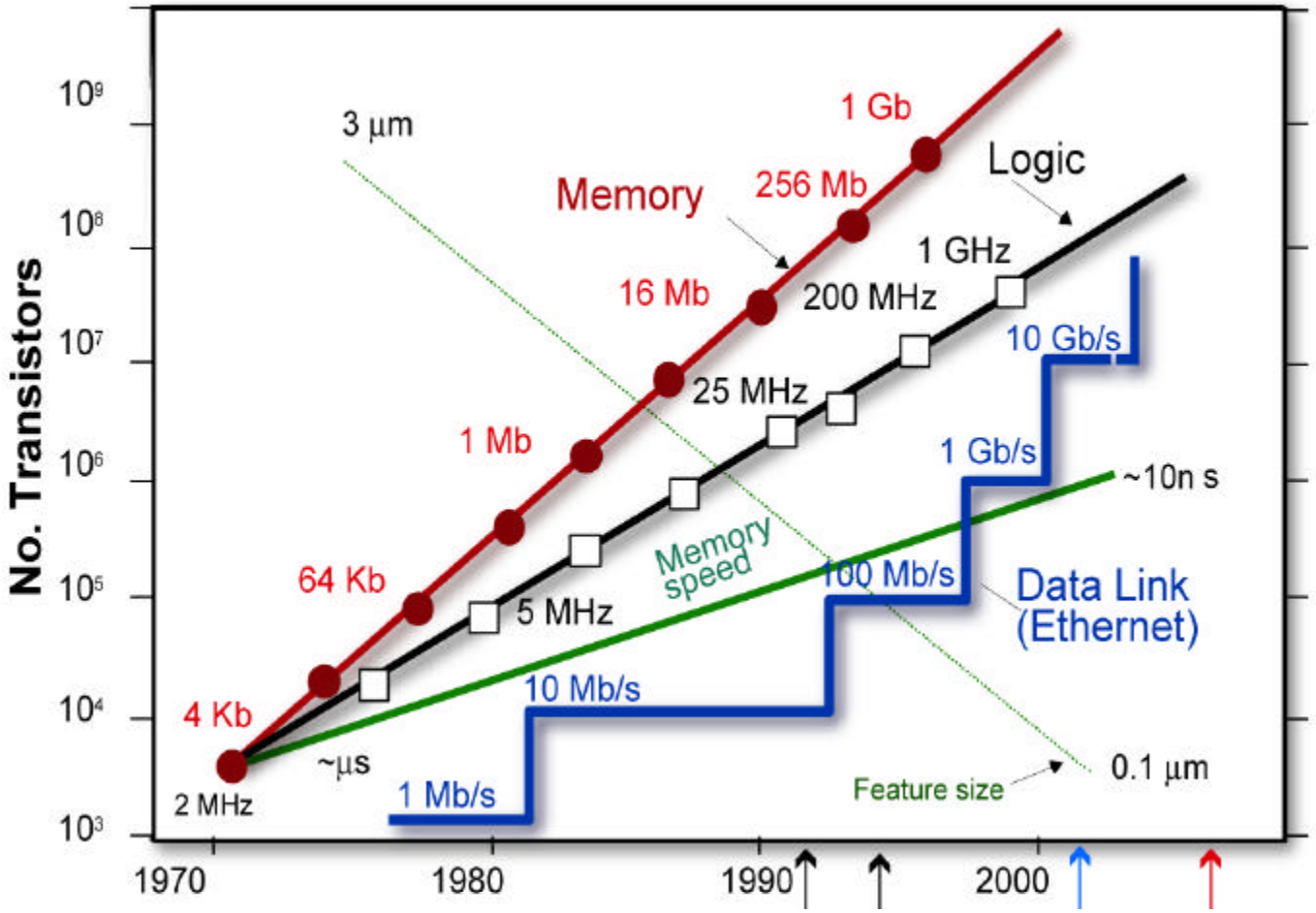


Babar

Track Segment Finder (x24)

Moore's Law

In 1965 Gordon Moore (Intel co-founder) observed that transistor densities on ICs were doubling every year.



S. Cittolin CERN/EP-CMD LECC Workshop 2002

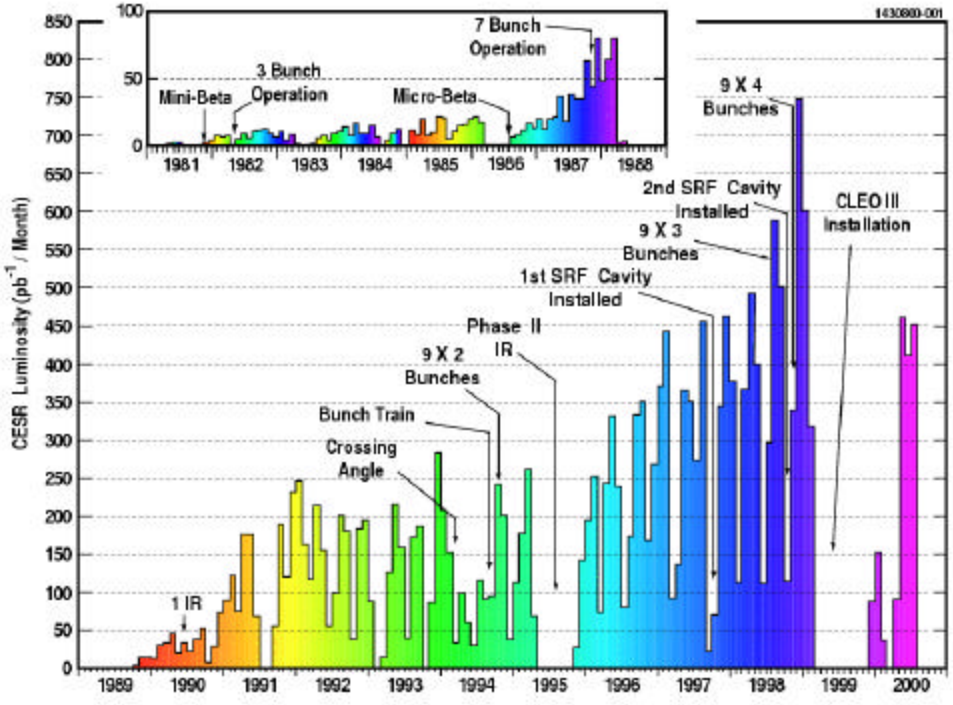
e+e- Luminosity Growth

- Luminosity at Upsilon(4S) has grown substantially over time:

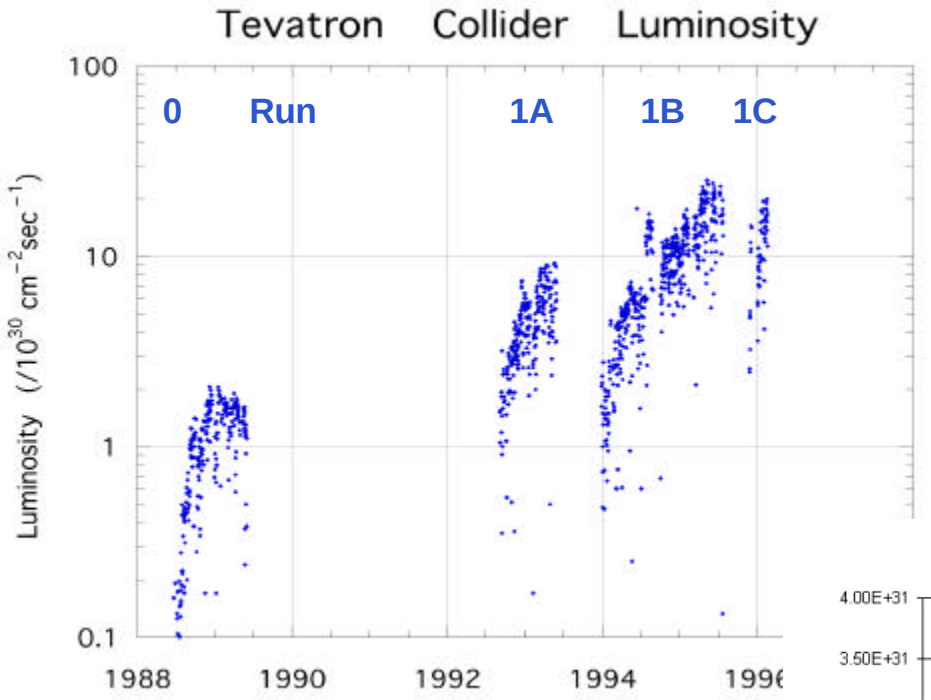
Accelerator	Year	Luminosity (fb^{-1}/month)
CESR (CLEO)	1982	0.010
CESR (CLEO)	1987	0.075
CESR (CLEO)	1992	0.250
CESR (CLEO)	1998	0.750
KEKB (Belle)	2002	6.660
PEP-II (Babar)	2002	8.617

- Factor of 25 from '82-'92
- Factor of 35 from '92-'02
  - Expect to increase at least another 25%
- Close to a factor of 1000 in 20 years
- Luminosity doubles about every 2 years
- Slightly slower than Moore's law

CESR Monthly Luminosity

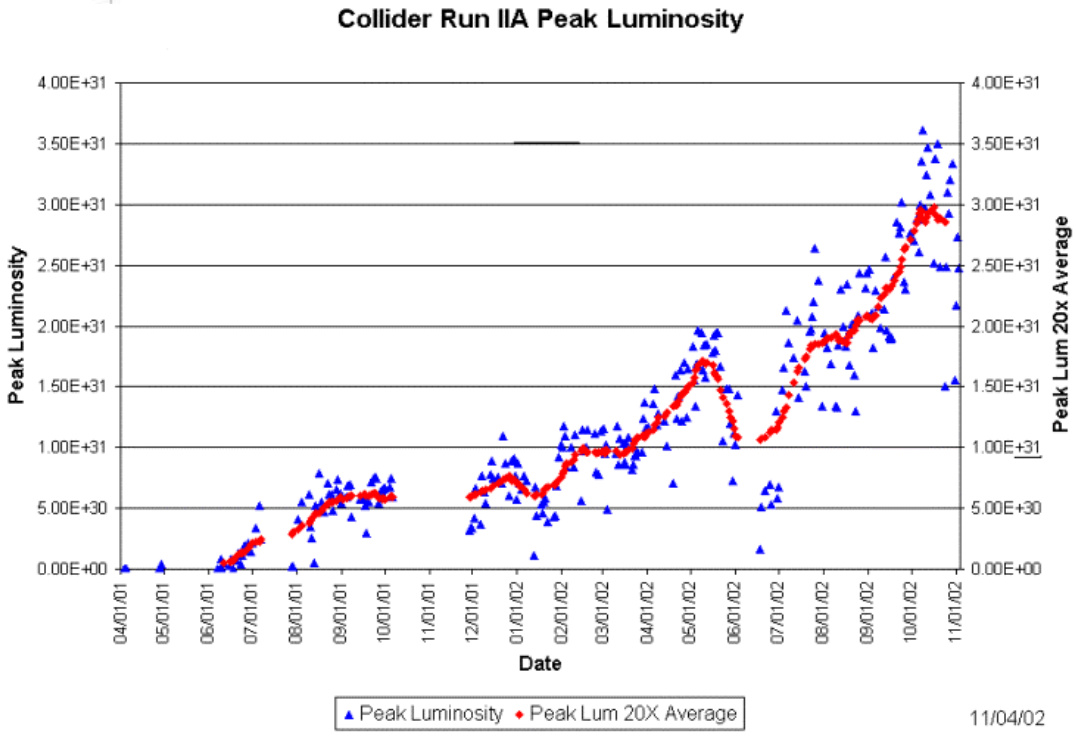


$p\bar{p}$ Luminosity Growth

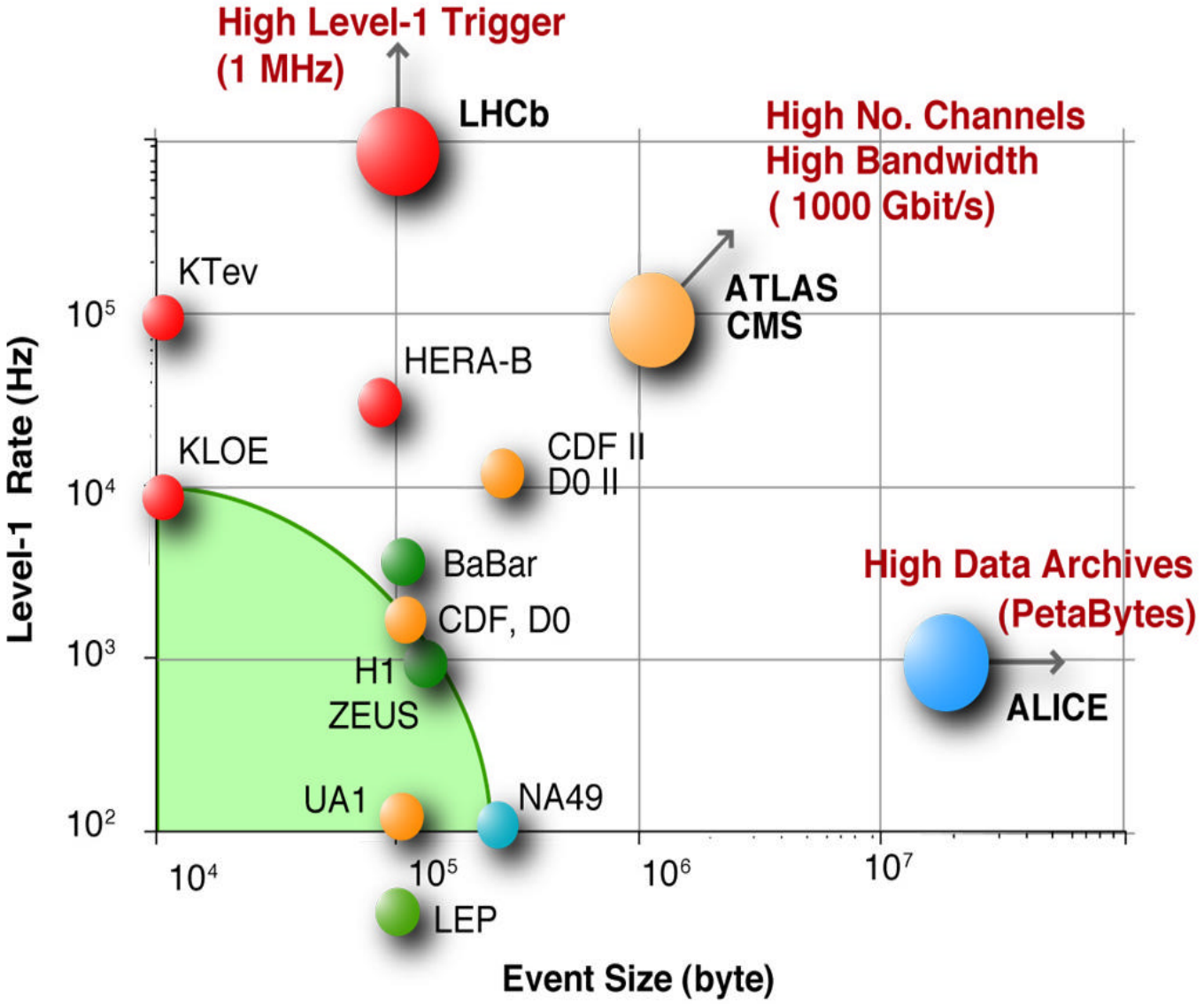


Accelerator	Year	Luminosity ($mb^{-1}s^{-1}$)
Tevatron (0)	1989	2.0
Tevatron (1A)	1993	9.0
Tevatron (1B)	1995	25.0
Tevatron (2A)	2002	36.0
Tevatron (2A)	2003	80.0
Tevatron (2B)	2006?	200-400
LHC	2008?	10,000

- Factor of ~10 in 10 years
  - Smaller than CESR
  - Trigger on lower Pt (expand B physics programs)
- Expect large increase going to LHC
  - Bigger than CESR to B-factory



Trigger and data acquisition trends



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Triggering in Future Experiments

Near Future Experiments (before 2010)

	Type	L1 In (MHz)	L1 Out (kHz)	L2 Out (kHz)	Ev Size (kB)	Bandwidth RO (GB/s)	L3 Out (Hz)
ATLAS	pp	40	100	NA	1000	10	100
CMS	pp	40	100	100	1000	100	100
LHCb	pp	40	1000	1000	200	4	200
BTeV	ppbar	7.6	80	8	100-200	800*	4000
CKM	K+-> p+nn	44MHz debunched beam				100?	100?
Minos	n oscill	19ns RF for 8ms spill, rep rate ~1s				40MB/s	few

* BTeV is read out before L1 trigger

With increasing link and switch capabilities less selection in hardware

Will Trigger PC boards start to get smaller again?

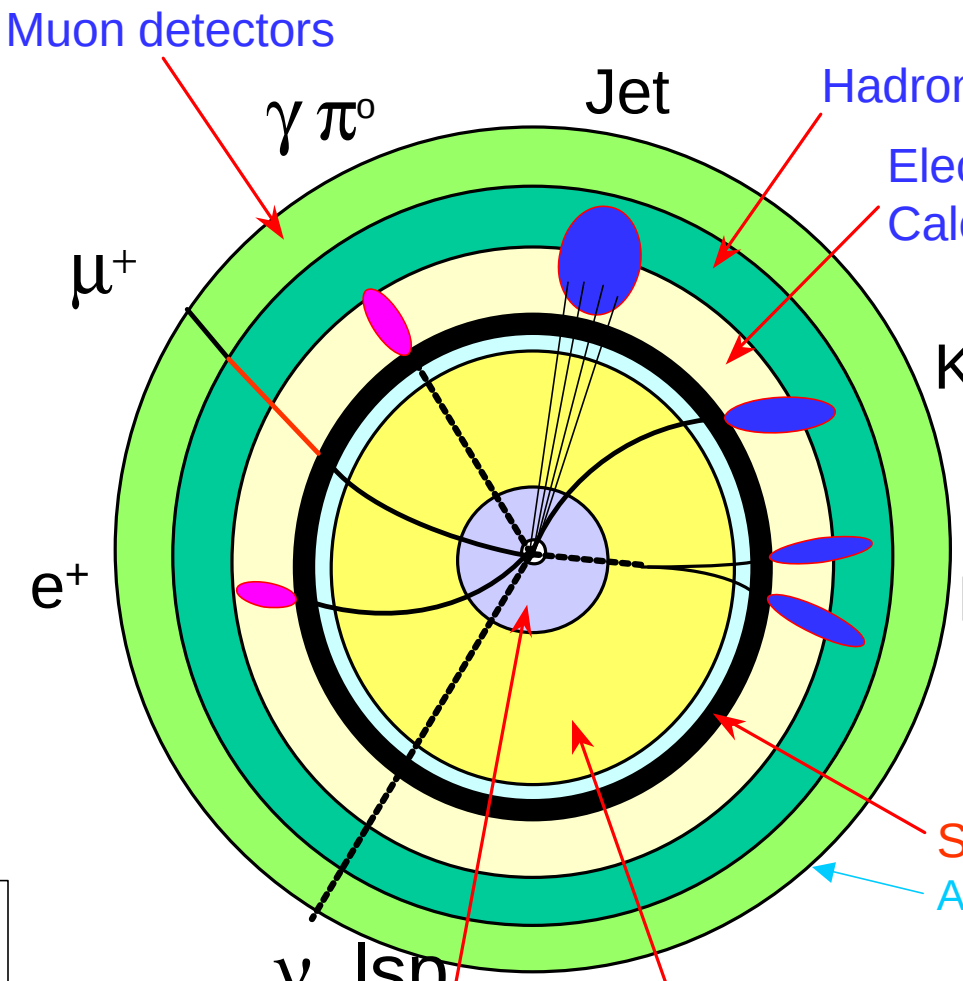
LHC Detector Schematic

Key

CMS and ATLAS

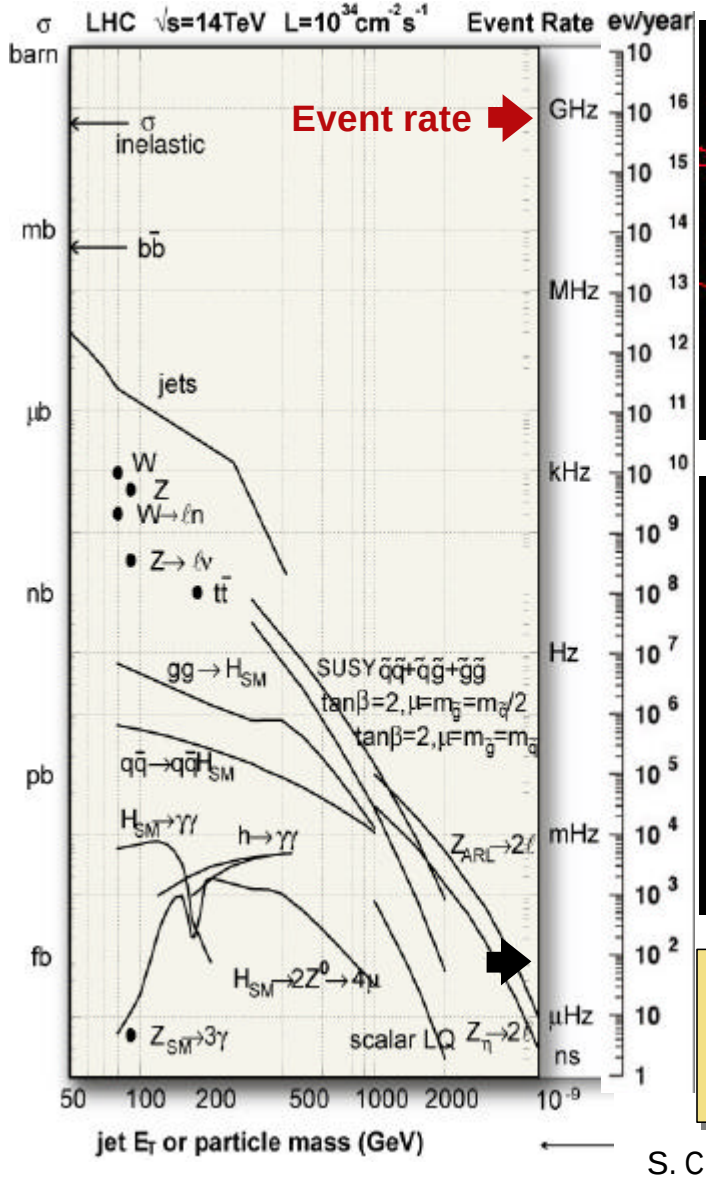
CMS

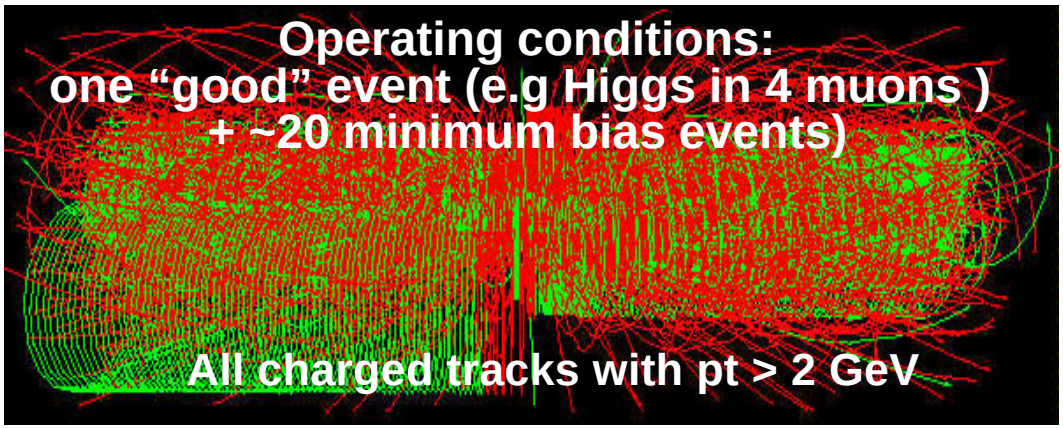
ATLAS

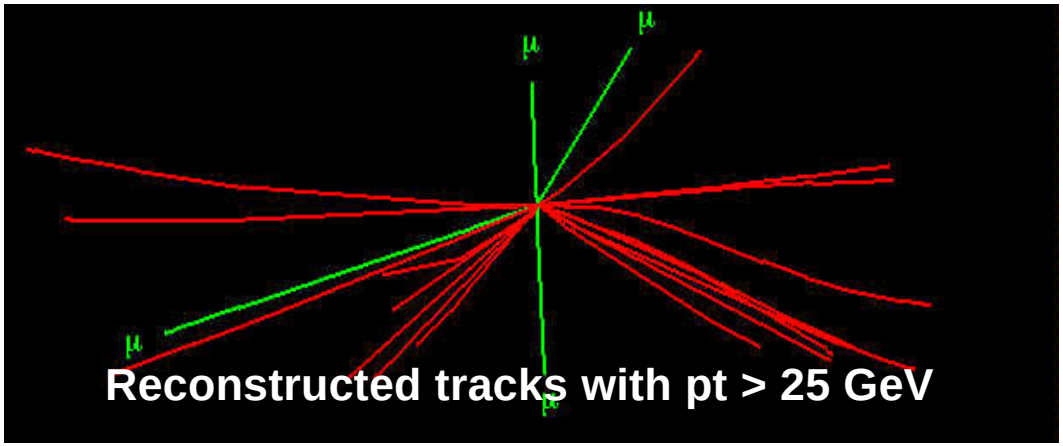


LHCb, BTeV and Numi look VERY Different

Collisions (p-p) at LHC







Event size: ~1 MByte
Processing Power: ~X TFlop

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ATLAS/CMS Trigger Rates

- Same challenges as Tevatron but higher energies, much higher luminosity ➔ more interactions/crossing (20-25)
- Cut on E_T and P_T to discriminate against QCD backgrounds
  - Higher E_T cuts than Tevtron needed
  - More boost ➔ don't loose efficiency
- Unprescaled High P_T trigger thresholds and rates:

	CDF L1		CDF L2		LHC L1	
	P_T Cut	Rate (HZ)	P_T Cut	Rate (Hz)	Pt Cut	Rate (Hz)
Single m	4 GeV/c	280	12 GeV/c	25	20 GeV	10k
Single e	8 GeV	240	16 GeV	30	30 GeV	20k
Single g	8 GeV	2400	18 GeV	60	30 (GeV)	20k
Single Jet	10 GeV	10K	90 GeV	10	300 (GeV)	200

CDF Rates for $2 \times 10^{32} cm^{-2} s^{-1}$, scaled from $3 \times 10^{31} cm^{-2} s^{-1}$ (no L2 μ)

LHC rates for $10^{34} cm^{-2} s^{-1}$, from N. Ellis, LECC Workshop 2002 at Colmar

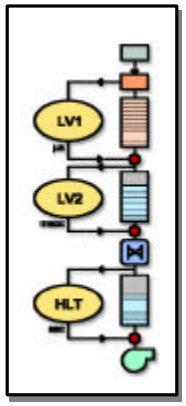
ATLAS and CMS Trigger Architecture

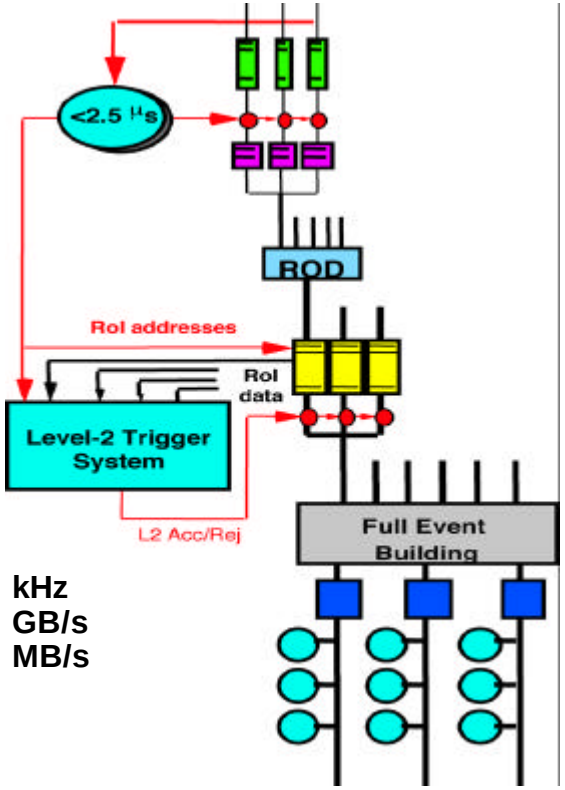
Large improvements in FPGA size, speed and link bandwidth

➔Only L1 trigger in custom hardware

➔No L2 trigger for CMS

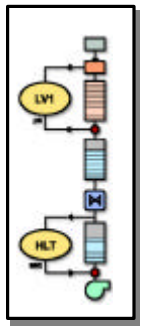
ATLAS

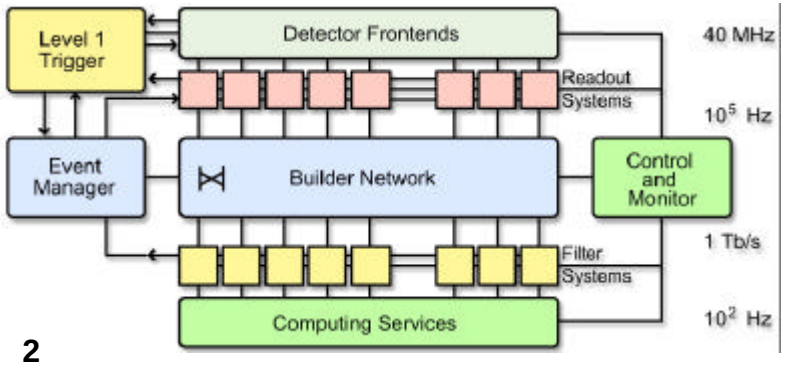




Levels	3	
LV-1 rate	100	kHz
Readout	10	GB/s
Storage	100	MB/s

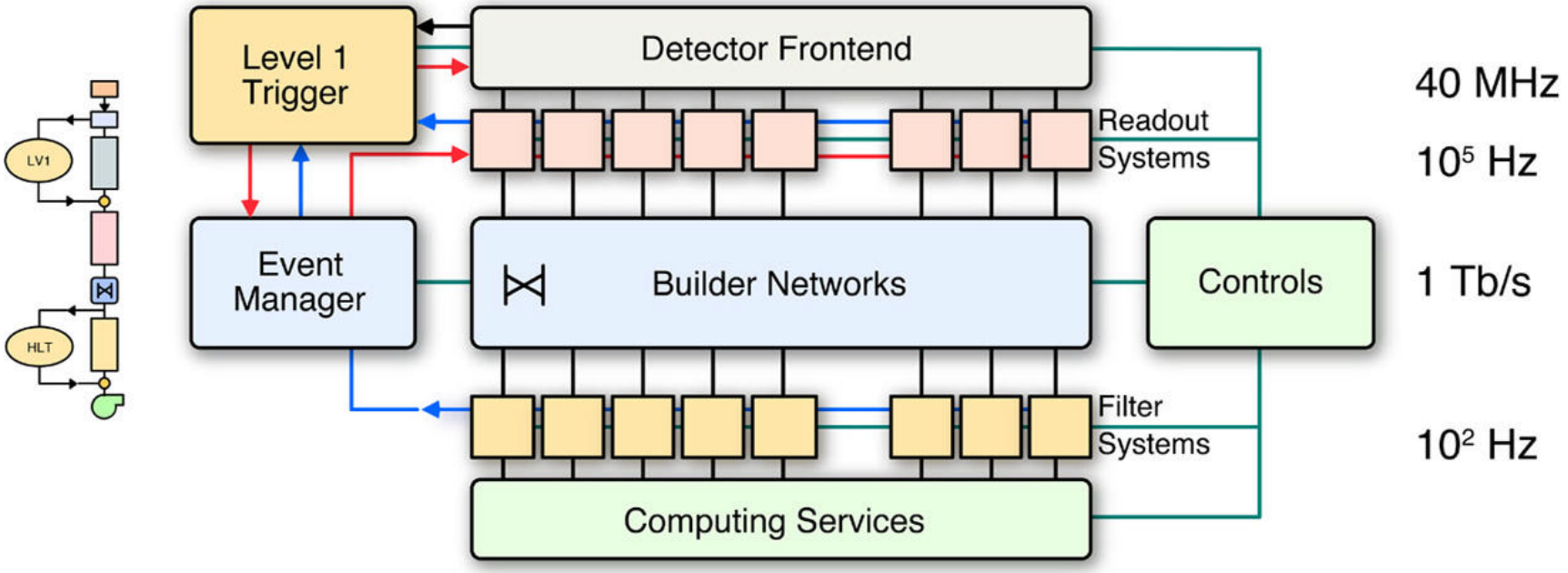
CMS





Levels	2	
LV-1 rate	100	kHz
Readout	100	GB/s
Storage	100	MB/s

CMS DAQ/Trigger Structure

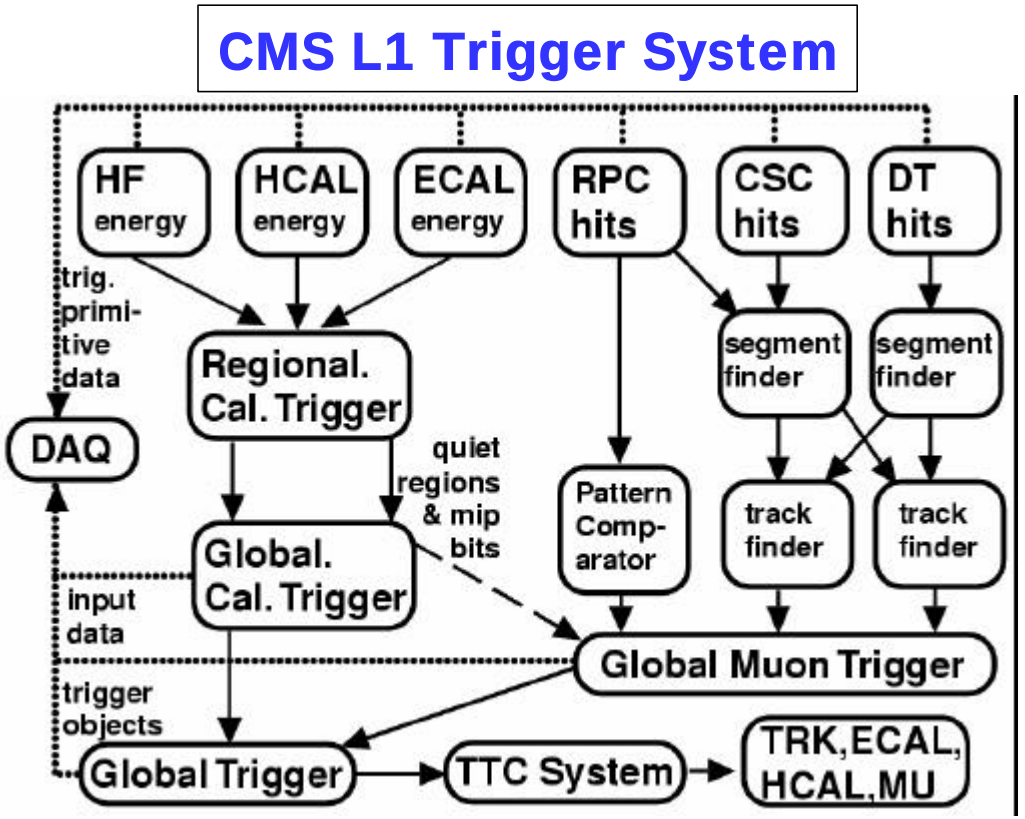


Collision rate	40 MHz
Level-1 Maximum trigger rate	**100 kHz(*)**
Average event size	**~ 1 Mbyte**
Event Flow Control Mssg/s	~ 10^6

No. of In-Out units	~ 500
Readout network bandwidth	**~ 1 Terabit/s**
Event filter computing power	**~ 5 TFlop**
Data production	~ Tbyte/day
No. of PC motherboards	~ Thousands

ATLAS and CMS L1 Trigger

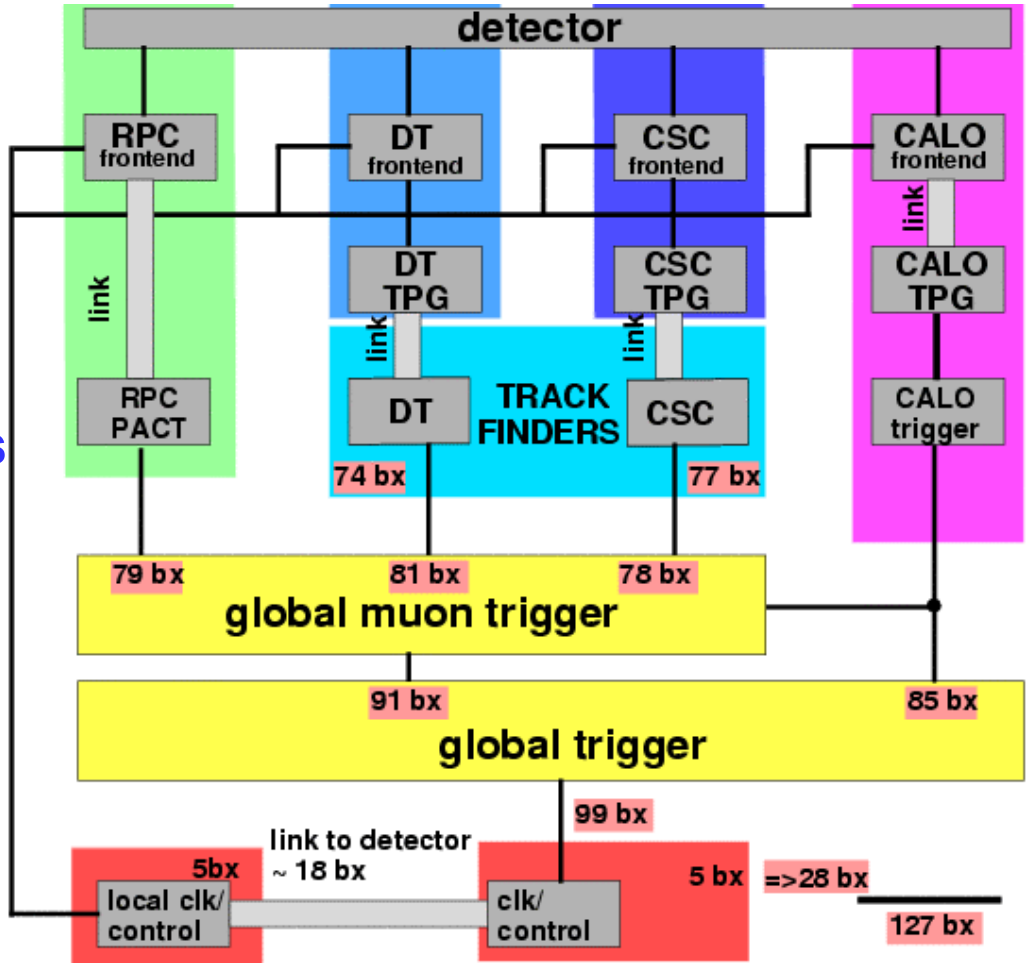
- CMS and ATLAS L1 triggers both use data from Calorimeters and Muon detectors
  - No data from inner trackers – very high track density
  - E_T of clusters for e/g/Jet triggers
  - Missing E_T for ν or SUSY LSP
  - P_T of Muon in flux return (CMS), air torroids (ATLAS)
- Same general functions as CDF/D0 Run 1 L1 Triggers
  - Better muon P_T
  - More sophisticated algorithms
  - Many more channels to handle



CMS L1 Latency

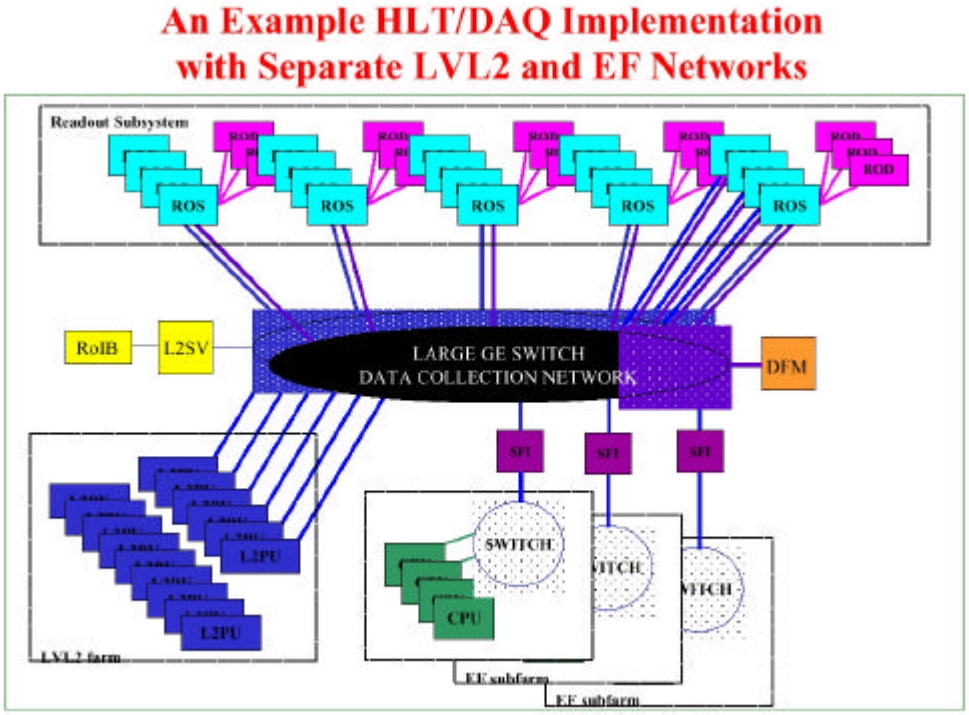
Budget of 128bx =3.2ms

CDF/D0 (30-42bx) ~ 4-5.5ms

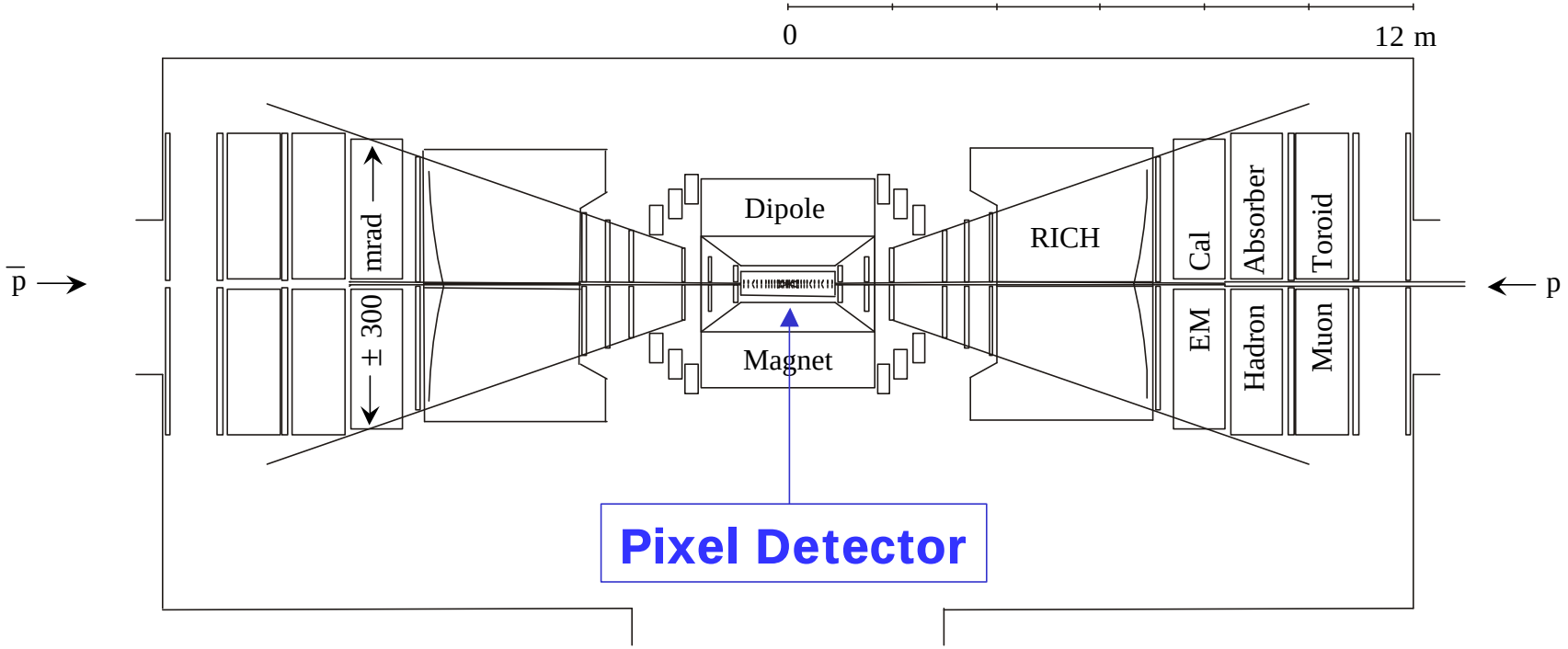


Atlas L2: Regions of Interest

- L2 Trigger uses same data as goes to L3
- On L1 subsystems store regional information about decision
  - On L1A, pass to Region of interest builder in L2
  - Fetch complete detector data only for Regions of Interest (ROI). Data remains in buffers of readout system
  - Make fast decision in L2 Processor farm. Reduce rate by factor of 10
- ROI builder gathers packets from different parts of detector and align to same even. Then pass to farm.
- Links: S-Link and/or GB ethernet



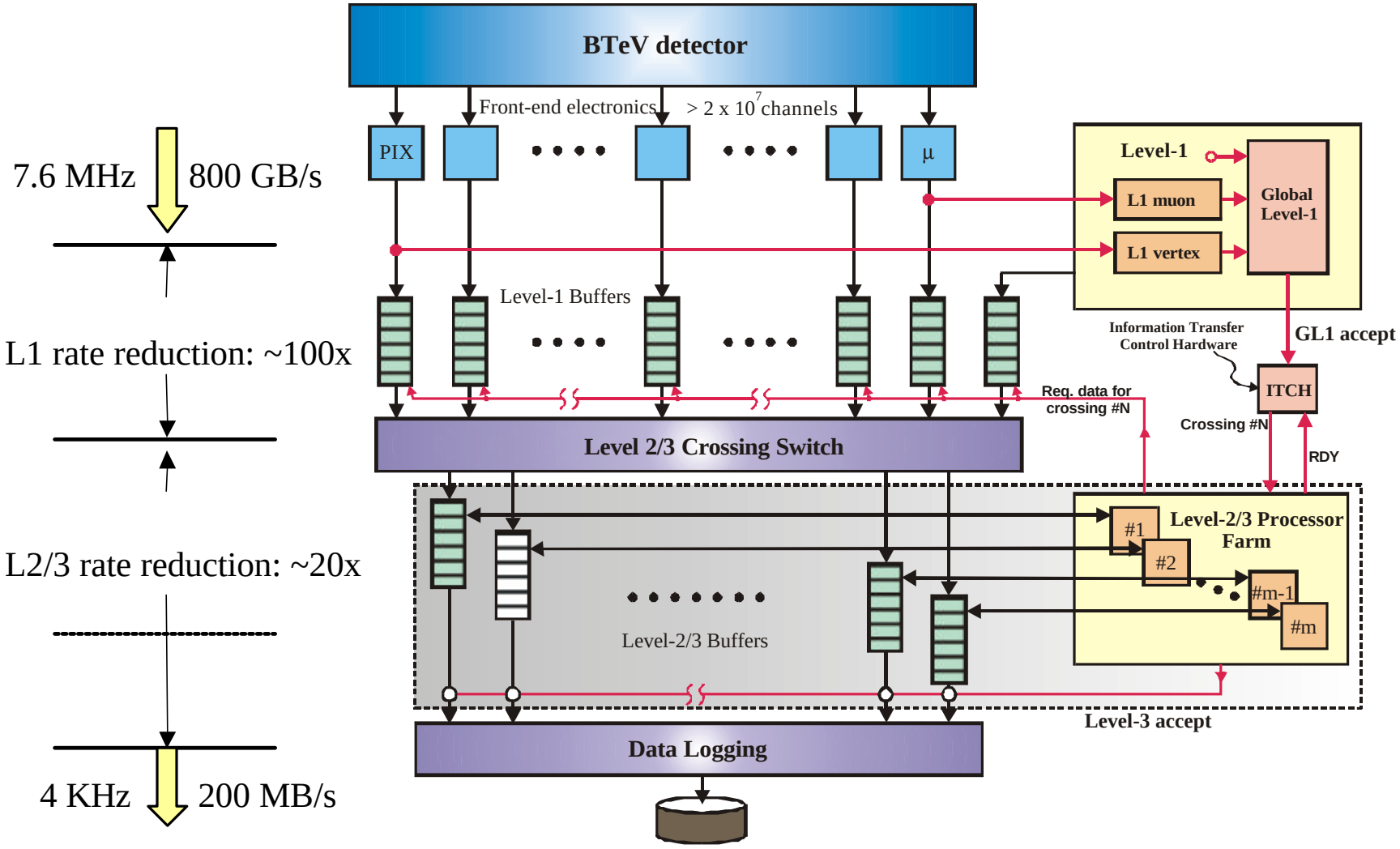
BTeV Detector



BTeV and LHCb: experiments dedicated to B physics

- **Large production at small angle relative to beamline (large |h|)**
- **Fixed target like geometry with dipole at collision region**
- **Goal to have much higher efficiency for B decays than High Pt detectors (CDF, D0, CMS, Atlas)**

BTeV Trigger and DAQ



Read data in memory before L1 decision: total of 400 Gbytes for L1, L2, L3 Buffers

BTeV Trigger

L1 Vertex Trigger uses data from pixel detector to select events with detached vertices (long lifetimes) using a combination of FPGAs and DSPs on custom boards .

L1 Muon Trigger provides alternate path for $B \rightarrow J/\psi + X$ with higher efficiency

- Use to measure efficiency of vertex trigger
- Also for useful for $B_S \rightarrow J/\psi + X$ in its own right

L1 Buffers may be managed as a circular buffer or as RAM. Optimization not complete

L2 and L3 Triggers implemented in commodity processors (eg Linux PCs)

- L2 seeded of tracks found at L1, improved fit to L1 tracks
- L3 full event data available
- Write only reconstructed data to tape, raw data only stored for a prescaled subset

Event Size	100-200kBytes
Number of 1Gb/s Links	5000
Number of L1 DSPs	2500
Number of L2/3 Processors	2500

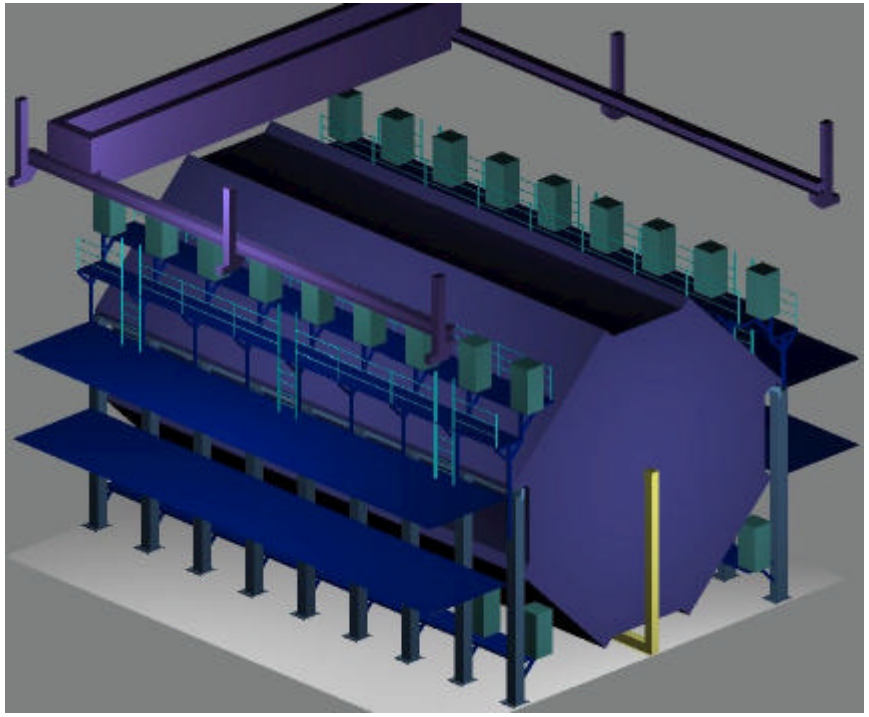
L2/L3 Trigger Performance Overview

Trigger Level	Trigger Parameters			
	Input Rate	Output Rate	Reduction Factor	Processing Time
Level 2 refined tracking, vertex cut	75KHz 100KB/event 8 GB/s	7.5KHz 100KB/event 800 MB/s	10	13ms
Level 3 uses full event data	7.5KHz 100KB/event 800 MB/s	4KHz 50KB/s 200MB/s	2	130ms

- L2 and L3 triggers are implemented in the same hardware, a PC Farm
- L2 Uses tracking information to look for detached vertices and detached tracks
- L3 does the full reconstruction and writes DSTs (similar to traditional offline)

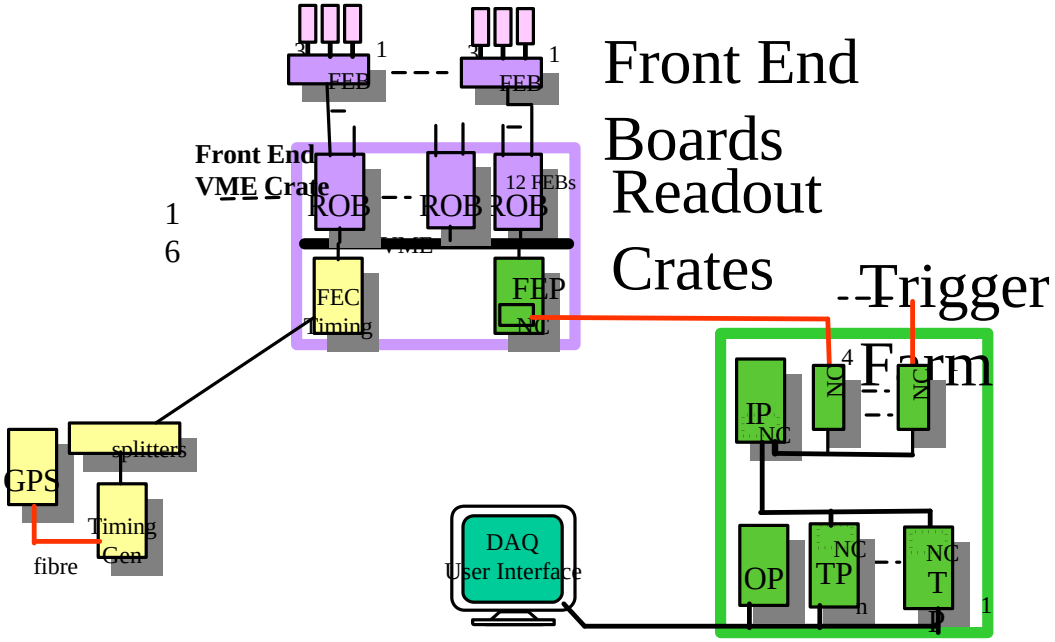
MINOS Far Detector

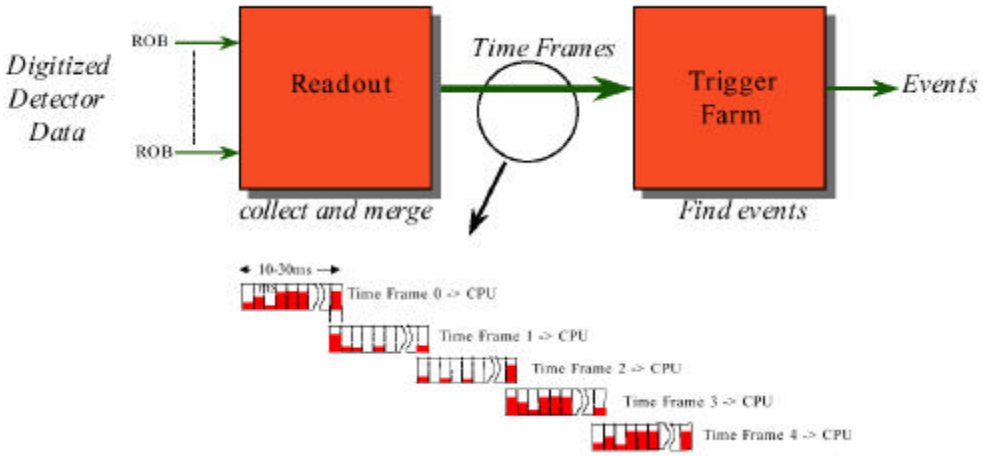
- Two detectors – near and far (730km separation)
- 8m Octagonal Tracking Calorimeter
- 486 layers of 2.54cm Fe
- 2 sections, each 15m long
- 4cm wide solid scintillator strips with WLS fiber readout
- 25,800 m^2 active detector planes
- Magnet coil provides $\langle B \rangle \approx 1.3T$
- 5.4kt total mass



Half of the MINOS Detector

MINOS Readout and Trigger





Two detectors – near and far (730km separation)

- time synch date <1ms (GPS)

No hardware trigger

Beam structure:

- **~10ms spill at ~1Hz**
- **53MHz structure within spill**

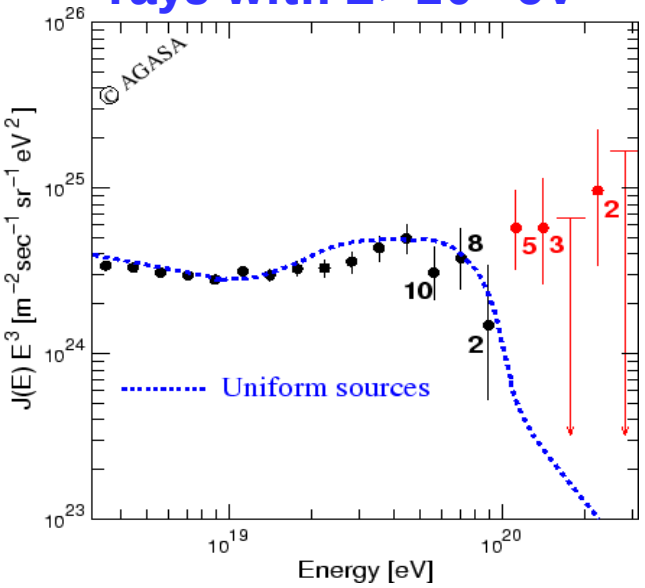
Continuous digitization at 53MHz

Readout into Trigger farm in overlapping ~4ms long frames of data

Readout rate: 40MB/s

Pierre Auger Observatory

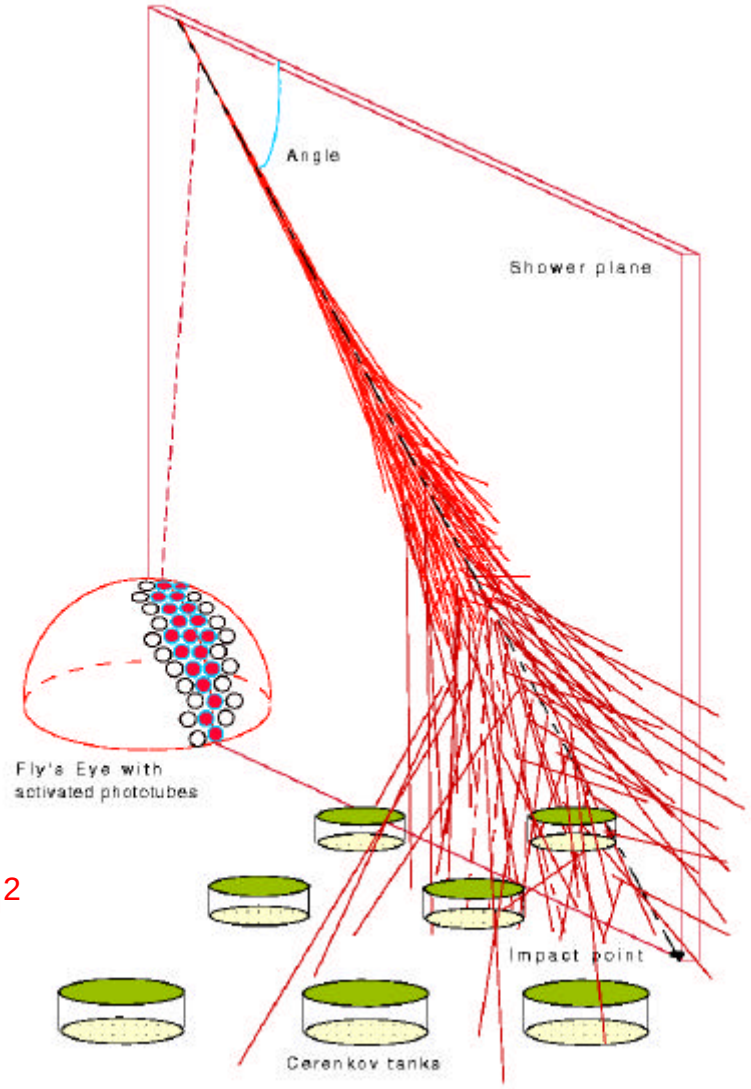
Search for Origin of cosmic rays with E>10^{20}eV



Rate ~ 1 / km^2 / sr / century above 10^{20} eV!

Large scale detector:

- ✓ 1600 Cherenkov tanks, covering 3000 km^2
- ✓ 24 Fluorescence Detector telescopes



Auger Cerenkov Stations

- Highly Distributed Particle physics detector
- Autonomous systems at each detector
  - Communicate via wireless technology
  - Timing via GPS (~10ns)
  - Cannot trigger globally
  - Two FADC (gain factor of 8) at 40MHz into buffer on each tube
- Backgrounds
  - PMT noise few kHz/PMT
  - Cosmics ~ 3kHz/station

Auger Trigger

Four level trigger

Locally: L1 in hardware – 100Hz out

Locally: L2 in μ-controller – 20Hz

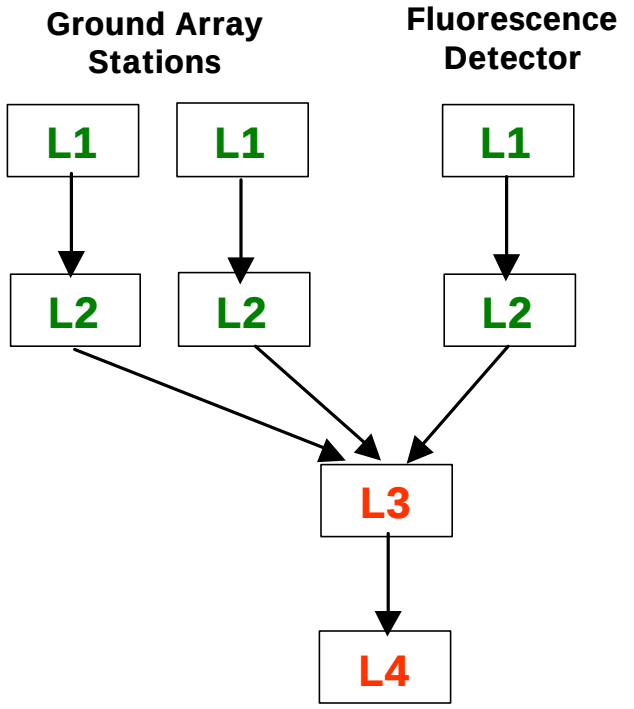
Transmit 3Bytes to control center on L2A

Globally: L3 and L4 in processors at control center

Data buffered locally to be retrievable after L3 even for un-triggered station

L1 Algorithm multiple time slices over threshold (eg 2 counts in low FADC range) in a sliding window (eg 4 time bins out of 240)

- Other algorithms look for single muons and Gamma Ray bursts
- Initially developed ASIC solution for low cost and power
- Decreasing FPGA costs: implemented in Altera ACEX EP1K100QI208-2. Algorithm in VHDL.
- In use: 40 station test array in Argentina

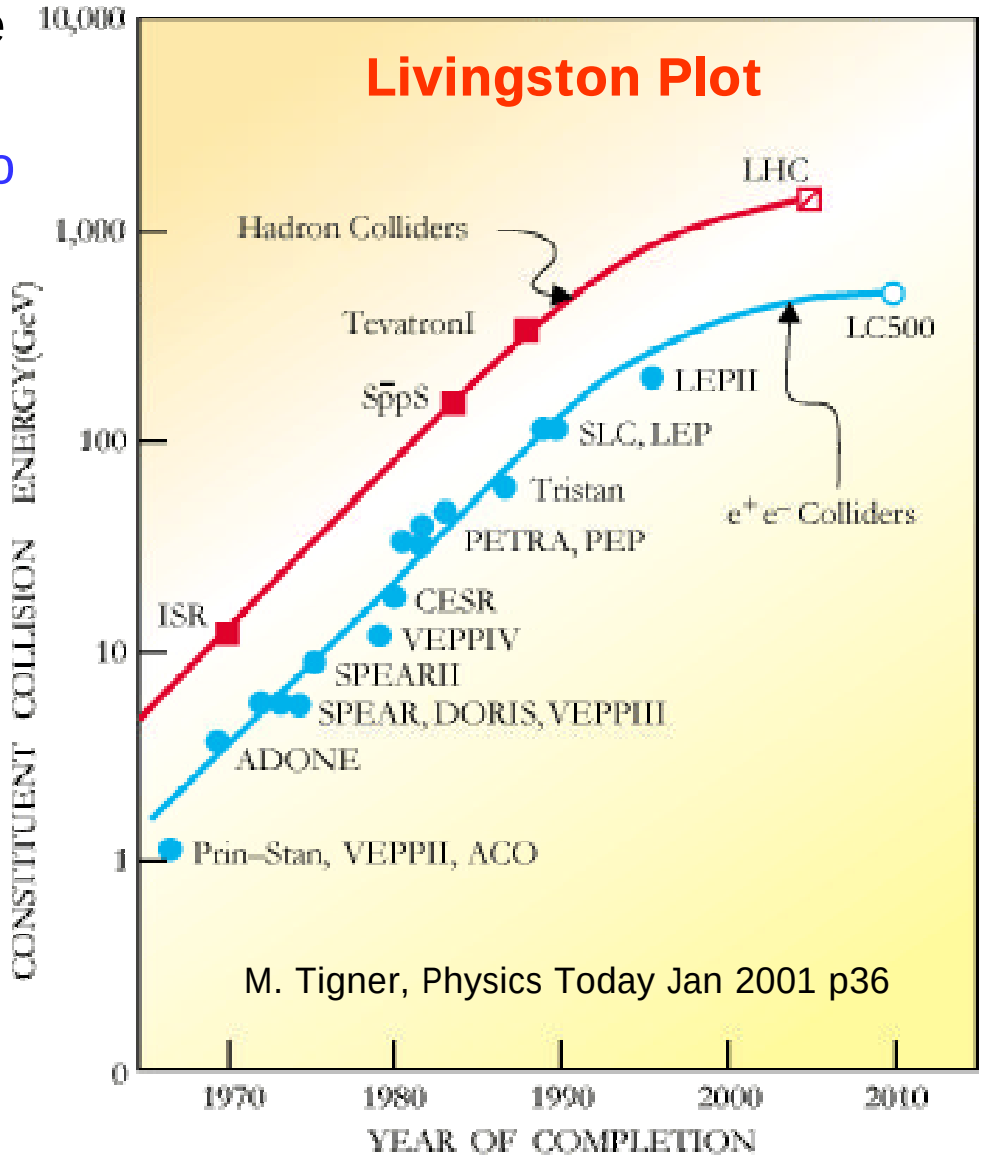


Send average of 500b/s from each ground station

Future Accelerators

What will trigger systems look like in the future?

- Accelerator energy continues to grow… however rate of change may be decreasing
- Processing power, network bandwidth and storage media are all growing faster than increases in luminosity
- Trend is toward fewer (zero?) hardware levels
- Future Machines
  - Linear Collider (500-1000 GeV)
  - Super B-Factory ($10^{36} cm^{-2} s^{-1}$)
  - ν factory?
  - Muon Collider?
  - VLHC pp at 40-200 TeV



Linear Colliders

Low Beam X-ing Rate for Either Tesla or NLC/JLC

	Tesla	NLC/JLC
Rep Rate (Hz)	5	120
Bunch Spacing (ns)	337	1.4
Bunch/Pulse	2820	190
Pulse length (ms)	950	0.266
Average xing rate (kHz)	14	23

Trigger-less (hardware) design

- Tesla conceptual detector: readout detector continuously to L3 farm

Super Babar

- Bunch spacing is already essentially DC (<10ns)
- Even with factor of 100 in luminosity the general character stays the same although slow calorimeters (CsI with Tl doping) might start to see pile-up
- Given a 10 year minimum timescale it seems likely that current schemes with a L1 hardware trigger and L3 farm would work.

Concluding Remarks

- Trend in trigger design over the past 20 years has been to greater complexity in hardware triggers
- With the increased capabilities (and decreased cost) of Ethernet, PCs, and Network switches, the complexity of custom hardware may decrease
- Corollary: HEP no longer is at cutting edge of electronics bandwidth
- The trend toward ASICs seem to have slowed
  - Use for very high volume (rare on trigger)
  - Use for special radiation environment (only first data formation for trigger)
  - Not as flexible in addressing un-forseen needs/desires